TD2115M
Product Specification

3GPP NB-IOT Release 14
LTE Category NB1
SiP Module

Version: 0.3

CONNEGENCE TECHNOLOGY CO., LTD.
Email: wyq@connegence-iot.com

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DOCUMENT HISTORY

The next table gives an overview of the changes to the document

DATE	VERSION	CHANGE	AUTHOR
May. 31. 2018	0.1	Preliminary	Vic Yang
July. 05. 2018	0.2	Update Table 4-1	Vic Yang
Sep. 25.2018	0.3	Revise Chapter 8 and Chapter 10	Vic Yang

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1 OVERVIEW

1.1 INTRODUCTION

TD2115M is highly integrated NB-IoT SiP module, including most power efficient IoT chip, RFFE, 38.4MHz TCXO, 32KHz XTAL, PMU and minimal set of external components. It is the smallest LTE category NB1 (Rel-14) module on the market and designed to meet the essential LTE connectivity for M2M and IoT applications.

It features compact size, ultra-low power consumption, extended coverage and enhanced RF performances with the miniature LGA form factor (14.0 x 14.0 x 1.85mm, 52-pin). It provides the cost effective and size sensitive solution to help customers to quick develop their devices for the strong growth in the NB-IoT market.

The operation band of TD2115M is flexible from 698 to 2180MHz. It mainly supports the following 3GPP bands.

Table 1-1 : Operation Bands of TD2115M

LTE Band	UL (MHz)	DL (MHz)	DUPLEX MODE
1	1920 - 1980	2110 – 2170	H-FDD
3	1710 -1785	1805 - 1880	H-FDD
5	824 - 849	869 – 894	H-FDD
8	880 – 915	925 - 960	H-FDD
20	832 - 862	791 – 821	H-FDD
28	703 - 748	758 - 803	H-FDD

1.2 KEY FEATURES

Table 1-2 : Key Features of TD2115M

Item	Description	Specification
Form Factor	LGA	52-PIN
Physical Features	Dimension	14.0mm x 14.0mm x 1.85mm
	Weight	< 2g
Operating Frequency	Band	B1/B3/B5/B8/B20/B28

Data Rate	Single-Tone	Max. DL: 24kbps / UL: 16kbps
	Multi-Tone	Max. DL: 24kbps / UL: 54kbps
Application Interface	USIM	Support external 3.0V or 1.8V USIM card
	UART	Main port: - AT command and data transmission, supporting 9600bps baud rate - Firmware upgrade, supporting 115200bps baud rate Debug port: - Debug and diagnostic information - Only support 921600bps baud rate for debug log
	SPI	Support external 3.3 or 1.8V serial flash
	I2C	Standard-mode bi-directional bus
	ADC/DAC	10-bit ADC and 10-bit DAC
	RSTB	Reset the module
	RF_ANT	Connect to antenna terminal with 50Ω impedance control
Data Service	Internet Protocol	IPv4/IPv6/UDP/CoAP/LwM2M/Non-IP DTLS/TCP
Programming	Firmware Upgrade	Main port UART or FOTA
Power Supply	VBAT	3.1V ~ 4.2V, typical 3.6V
Current Consumption	Active	TX: 50mA @ 0dBm RX: 60mA
	Standby (Idle)	2mA
	Deep Sleep (PSM)	5uA
Environment	Operating Temperature	-30 ~ 75℃
	Extend Temperature	-40 ~ 85℃

1.3 APPLICATION

- Smart Grid
- Smart Metering
- Smart Parking
- Traffic Management and Monitoring
- Security and Asset Tracking
- Home and Industrial Automation
- Agricultural and Environmental Monitors

1.4 FUNCTIONAL BLOCK DIAGRAM

The functional block diagram and interfaces of TD2115M are illustrated in the figure below. The major functional units of TD2115M contain the following parts.

- Main chip: Baseband controller, Power Management Unit, RF transceiver and analogue
- RFFE: RF switch, transmitter filter, receiver filter, power amplifier and RF matching circuit
- Power unit: LDO, DC-DC converter, load switch
- Clock unit: 38.4MHz TCXO and 32kHz Crystal

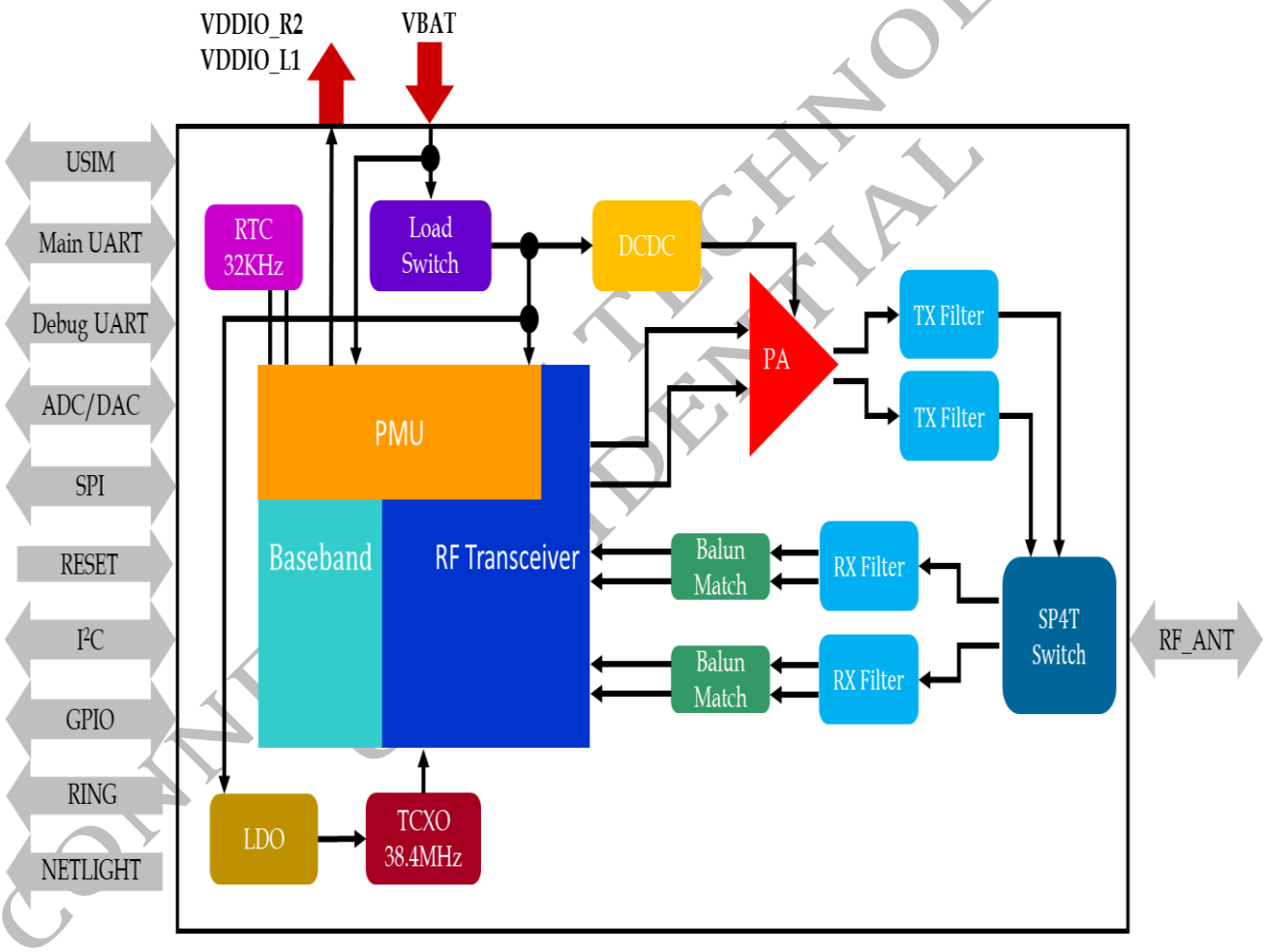

Figure 1-1 : Functional Diagram

1.5 OPERATING MODES

TD2115M has three operating modes, which determine available functionality for different levels of power-saving.

Table 1-3 : Overview of Operating Modes

Operating Mode	Function Description
Active	In Active mode, all functionality of the chip is available and all processors may be executing firmware. Radio transmission and reception is performed whilst in this mode. Transitions to Standby mode and Deep-Sleep mode can only be initiated when in Active mode.
Standby	In Standby mode, all processors are inactive, but all peripherals (including DMA and embedded Flash) can be active. The system clock is active and power consumption is reduced via clock-gating and power-gating. Standby mode is entered when all processors are executing a wait-for-interrupt (WFI) instruction.
Deep-Sleep	In Deep-Sleep mode, only the32.768kHz RTC and certain peripherals are running. The chip can be moved to active state by an RTC interrupt or by an external event through the peripherals that are using the RTC. This mode is entered by all processors setting the “sleep-deep” bit and then executing a WFI instruction.

2 PIN DEFINITION

2.1 PIN OUTLINE

TD2115M is a LGA package and equipped with 52 pins. The system interfaces are contained power supply, UART interfaces, RESET interface, USIM interfaces, ADC interfaces, NETLIGHT, RING signal, GPIO interfaces, RF interface and Reserved interfaces on these pins.

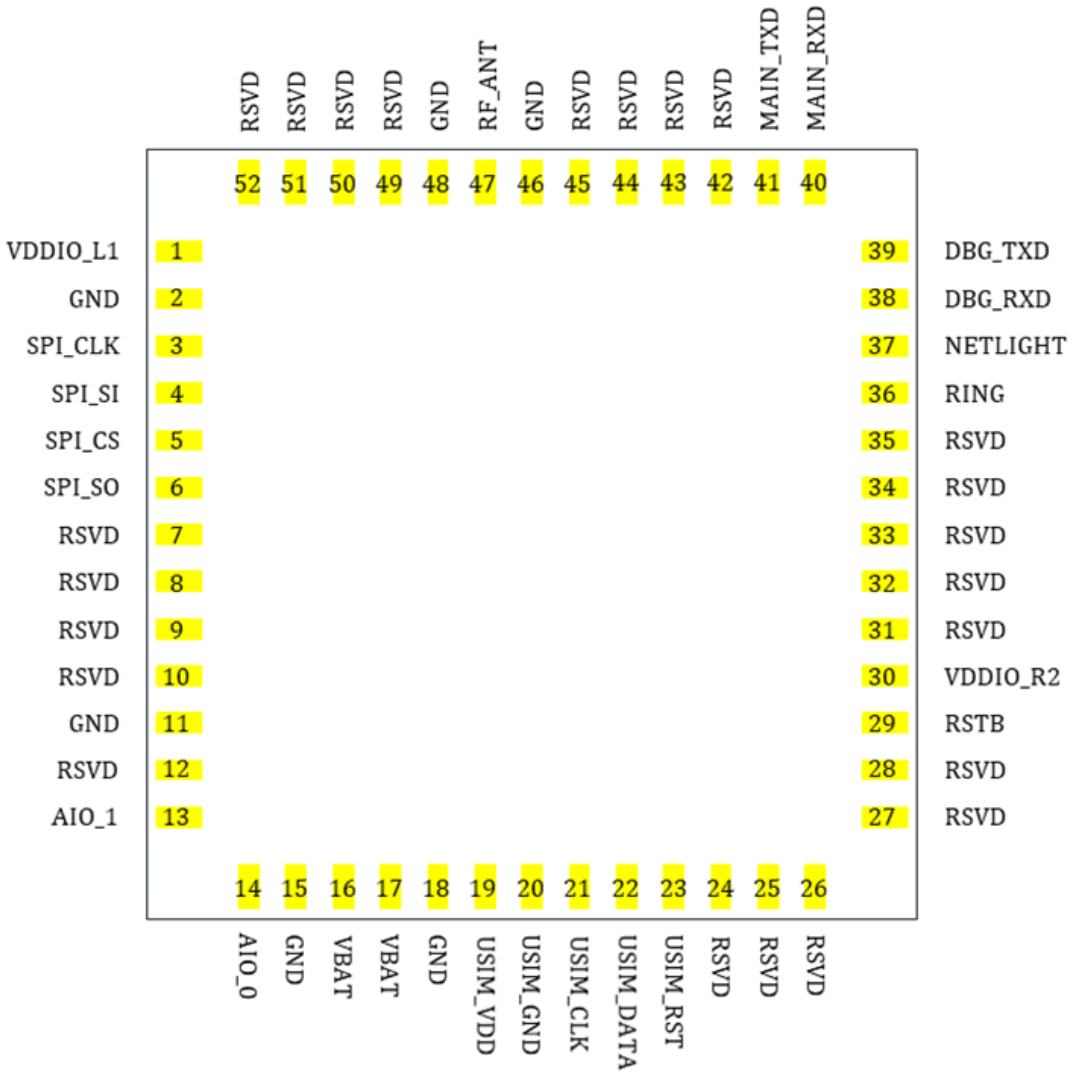

Figure 2-1 : Pin Assignment (TOP VIEW)

2.2 PIN DESCRIPTION

The system interface of TD2115M is through the LGA pad on the bottom of the PCB. The following table indicates the pin definition and description.

Table 2-1 : Pin Definition and Description

Pin NO	Pin Name	Type	Description	Note
1	VDDIO_L1	PO	I/O power supply output	This pin is S/W configurable. It is disabled by default.
2	GND	GND	Ground connection	Must be connected to ground.
3	SPI_CLK	DI	Serial data clock input	Support external serial flash. Leave it open if not used.
4	SPI_SI	DI	Serial data input	Support external serial flash. Leave it open if not used.
5	SPI_CS	DI	Chip select	Support external serial flash. Leave it open if not used.
6	SPI_SO	DO	Serial data output	Support external serial flash. Leave it open if not used.
7	RSVD	-	Reserved pin for future use	Leave it open.
8	RSVD	-	Reserved pin for future use	Leave it open.
9	RSVD	-	Reserved pin for future use	Leave it open.
10	RSVD	-	Reserved pin for future use	Leave it open.
11	GND	GND	Ground connection	Must be connected to ground.
12	RSVD	-	Reserved pin for future use	Leave it open.
13	AIO_1	AIO	Analog input and output	Leave it open if not used.
14	AIO_0	AIO	Analog input and output	Leave it open if not used.
15	GND	GND	Ground connection	Must be connected to ground.
16	VBAT	PI	Main power supply input	Must be connected to external power supply. 500mA minimum load capability is required.
17	VBAT	PI	Main power supply input	Must be connected to external power supply. 500mA minimum load capability is required.
18	GND	GND	Ground connection	Must be connected to ground.
19	USIM_VDD	PO	USIM power supply output	1.8V or 3.0V power supply. Connect with a TVS diode for ESD protection
20	USIM_GND	GND	USIM card ground connection	Must be connected to ground.
21	USIM_CLK	DO	USIM clock signal	Connect with a TVS diode for ESD protection
22	USIM_DATA	DIO	USIM data signal	Connect with a TVS diode for ESD protection

23	USIM_RST	DO	USIM reset signal	Connect with a TVS diode for ESD protection
24	RSVD	-	Reserved pin for future use	Leave it open.
25	RSVD	-	Reserved pin for future use	Leave it open.
26	RSVD	-	Reserved pin for future use	Leave it open.
27	RSVD	-	Reserved pin for future use	Leave it open.
28	RSVD	-	Reserved pin for future use	Leave it open.
29	RSTB	DI	Reset the module	Pull up internally. Active low.
30	VDDIO_R2	PO	Power supply for external circuit	3.0V power supply. Leave it open if not used.
31	RSVD	-	Reserved pin for future use	Leave it open.
32	RSVD	-	Reserved pin for future use	Leave it open.
33	RSVD	-	Reserved pin for future use	Leave it open.
34	RSVD	-	Reserved pin for future use	Leave it open.
35	RSVD	-	Reserved pin for future use	Leave it open.
36	RING	DO	Ring indication	3.0V power domain. Leave it open if not used.
37	NETLIGHT	DO	The indication of network status	3.0V power domain. Leave it open if not used.
38	DBG_RXD	DI	UART serial data input	Used for debug and diagnostic information. 3.0V power domain. Leave it open if not used.
39	DBG_TXD	DO	UART serial data output	Used for debug and diagnostic information. 3.0V power domain. Leave it open if not used.
40	MAIN_RXD	DI	UART serial data input	Used for AT command and firmware upgrade. 3.0V power domain.
41	MAIN_TXD	DO	UART serial data output	Used for AT command and firmware upgrade. 3.0V power domain.
42	RSVD	-	Reserved pin for future use	Leave it open.
43	RSVD	-	Reserved pin for future use	Leave it open.
44	RSVD	-	Reserved pin for future use	Leave it open.
45	RSVD	-	Reserved pin for future use	Leave it open.
46	GND	GND	Ground connection	Must be connected to ground.
47	RF_ANT	AIO	RF antenna port	50Ω impedance control is required. Connect with a TVS diode for ESD protection

48	GND	GND	Ground connection	Must be connected to ground.
49	RSVD	-	Reserved pin for future use	Leave it open.
50	RSVD	-	Reserved pin for future use	Leave it open.
51	RSVD	-	Reserved pin for future use	Leave it open.
52	RSVD	-	Reserved pin for future use	Leave it open.

Table 2-2 : I/O Definition

Type	Description
AIO	Analog input and output
AI	Analog input
AO	Analog output
DIO	Digital input and output
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
GND	Ground

3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATING

Table 3-1 : Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	+4.25	V
VDDIO_L1	-0.3	+4.25	V
VDDIO_R2	-0.3	+4.25	V
USIM_VDD	-0.3	+4.25	V
UART	-0.3	+4.25	V
RSTB	-0.3	+4.25	V
Voltage to Analog Pins	-0.3	+4.25	V
Voltage to Digital Pins	-0.3	+4.25	V

3.2 ENVIRONMENTAL REQUIREMENT

Table 3-2 : Environment Requirement

Parameter	Min.	Max.	Unit
Normal Operating Temperature Range	-30	+75	℃
Extended Operating Temperature Range	-40	+85	℃
Storage Temperature	-40	+90	℃
Operating Humidity	10	85	%
Storage Humidity	5	90	%

- Normal Operating Temperature Range: The functionality of module is met the 3GPP specification across the specified temperature range.
- Extended Operating Temperature Range: The functionality of module is normal across the specified temperature range. The deviation from 3GPP specification may occur.

3.3 ESD PROTECTION

Table 3-3 : Maximum ESD Rating

Parameter	Min.	Typ.	Max.	Unit
All Pins			±1	kV

- The module is sensitive to ESD. Require special precautions when handling.

3.4 RECOMMENDED OPERATION RATING

3.4.1 Power Supply

Table 3-4 : DC Characteristics of Power Supply

Parameter	Min.	Typ.	Max.	Unit
VBAT	3.1	3.6	4.2	V
VDDIO_L1 (1.8V)	1.7	1.8	1.9	V
VDDIO_L1 (3.3V)	3.2	3.3	3.4	V
VDDIO_R2 (3.0V)	2.9	3.0.	3.1	V
USIM_VDD (1.8V)	1.7	1.8	1.9	V
USIM_VDD (3.0V)	2.9	3.0.	3.1	V

3.4.2 UART Interface

Table 3-5 : DC Characteristics of UART Interface

Parameter	Min.	Typ.	Max.	Unit
Power Domain		VDDIO_R2		V
Low Level Input	-0.1*VDDIO_R2		0.2*VDDIO_R2	V
High Level Input	0.7*VDDIO_R2		1.1*VDDIO_R2	V
Low Level Output		0		V
High Level Output		VDDIO_R2		V
Leakage Current			±10	μA

3.4.3 USIM Interface

Table 3-6 : DC Characteristics of USIM Interface

Parameter	Min.	Typ.	Max.	Unit
Power Domain		USIM_VDD		V
Low Level Input	-0.1*USIM_VDD		0.2* USIM_VDD	V
High Level Input	0.7* USIM_VDD		1.1* USIM_VDD	V
Low Level Output		0		V
High Level Output		USIM_VDD		V
Leakage Current			±10	μA

3.4.4 SPI Interface

Table 3-7 : DC Characteristics of SPI Interface

Parameter	Min.	Typ.	Max.	Unit
Power Domain		VDDIO_L1		V
Low Level Input	-0.1* VDDIO_L1		0.2* VDDIO_L1	V
High Level Input	0.7* VDDIO_L1		1.1* VDDIO_L1	V
Low Level Output		0		V
High Level Output		VDDIO_L1		V
Leakage Current			±10	μA

3.4.5 RSTB Pin

Table 3-8 : DC Characteristics of RSTB Pin

Parameter	Min.	Typ.	Max.	Unit
Power Domain		VDDIO_R2		V
Low Level Input	-0.1* VDDIO_R2		0.2* VDDIO_R2	V
High Level Input	0.7* VDDIO_R2		1.1* VDDIO_R2	V
Pull-up Resistance		78		kΩ
Low Level Input Current			-10	μA
Low Level Reset Time	500			ns

3.4.6 NETLIGHT and RING Pin

Table 3-9 : DC Characteristics of NETLIGHT and RING Pin

Parameter	Min.	Typ.	Max.	Unit
Power Domain		VDDIO_R2		V
Low Level Output			0.1* VDDIO_R2	V
High Level Output	0.8* VDDIO_R2			V
Leakage Current			±10	μA

3.5 CURRENT CONSUMPTION

The supply current for various modes with operation at 25℃ and VBAT = 3.6V.

Table 3-10 : Current Consumption

Operating Mode	Description	Min.	Typ.	Max.	Unit
Deep-Sleep	Power Saving Mode			5	μA
Standby	Idle Mode		2		mA
Active	Transmit at 23dBm (B1)		220		mA
	Transmit at 23dBm (B3)		190		mA
	Transmit at 23dBm (B5)		210		mA
	Transmit at 23dBm (B8)		230		mA
	Transmit at 23dBm (B20)		210		mA
	Transmit at 23dBm (B28)		250		mA
	Transmit at 0dBm (B1/B3/B5/B8/B20/B28)		50		mA
	Receive		60		mA

4 RF SPECIFICATION

4.1 TRANSMITTER OUTPUT POWER

Table 4-1 : Transmitter Output Power

Band	Max.	Min.
B1	23dBm±2dB	< -40dBm
B3	23dBm±2dB	< -40dBm
B5	23dBm±2dB	< -40dBm
B8	23dBm±2dB	< -40dBm
B20	23dBm±2dB	< -40dBm
B28	23dBm±2dB	< -40dBm

4.2 RECEIVER SENSITIVITY

Table 4-2 : Receiver Sensitivity

Band	Condition	Typ.
B1	MCS-1, BLER<10%	-129dBm±1dB
B3		-129dBm±1dB
B5		-129dBm±1dB
B8		-129dBm±1dB
B20		-129dBm±1dB
B28		-129dBm±1dB

4.3 ANTENNA REQUIREMENT

Table 4-3 : Antenna Requirement

Parameter		Requirement	Unit
Frequency Range	Low Band	703 ~ 960	MHz
	High Band	1710 ~ 2200	
VSWR		<2	
Antenna Efficiency		40	%
Polarization		Linear	

Radiation Pattern	Omni-directional	
Input Impedance	50	Ω

5 DESIGN RECOMMENDATION

5.1 RESET

TD2115M can be reset by holding the RSTB pin low. The RSTB has an internal pull-up. The Reset state does not correspond to the lowest power consumption state of the module. The reset timing is illustrated in the table below.

Table 5-1 : Reset Timing Requirement

Pin Name	Pin No.	Min.	Typ.	Max.	Unit
RSTB	29	500			ns

The reference design of reset circuit is shown as below. It is recommended to have the following suggestions.

- An open drain driver from MCU is used to control RSTB pin.
- A button is used to control RSTB pin and firmware upgrade.
- Add TVS diodes for ESD protection and place it as close as possible to SW1.
- Add a capacitor to avoid button bouncing.

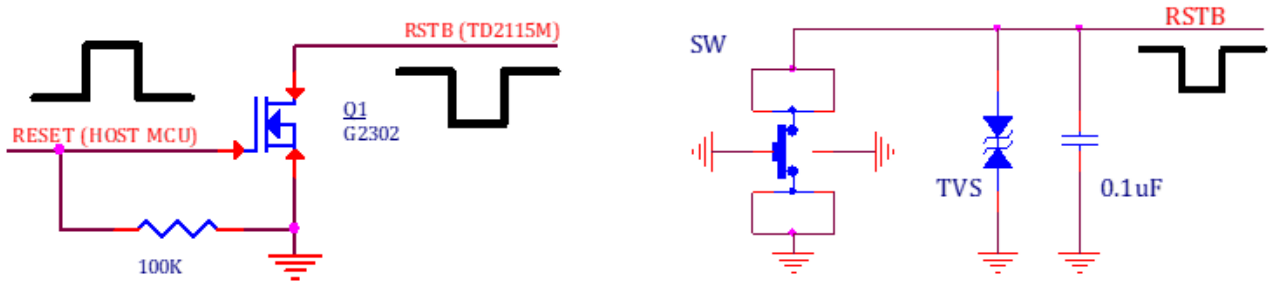

Figure 5-1 : Reference Design of RESET Circuit

5.2 UART INTERFACE

TD2115M has two UART interfaces for communication. One is main port used for sending AT command and another is debug port used for collecting debug message. The UARTs have programmable baud rates and are available in both Active and Standby modes.

Table 5-2 : UART Interface

Pin Name	Pin No.	Comment
MAIN_TXD	41	AT command and data transmission, supporting 9600bps baud rate. Firmware upgrade, supporting 115200bps baud rate. 3.0V power domain, depending on VDDIO_R2.
MAIN_RXD	40	

DBG_TXD	39	Debug and diagnostic information. Only support 921600bps baud rate for debug log. 3.0V power domain, depending on VDDIO_R2.
DBG_RXD	38	

The reference design of UART circuit is shown as below. It is recommended to have the following suggestions.

- Note that the UART logic level in circuit designing.
- Note that the UART connections between TD2115M and MCU.
- Reserve 0Ω resistors for the consideration of signal integrity.

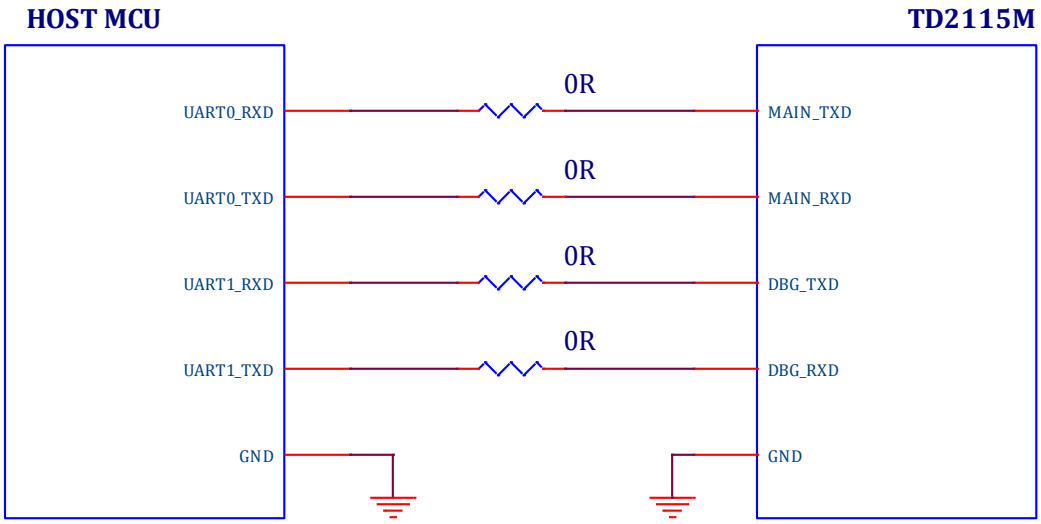

Figure 5-2 : Reference Design of UART Interface

5.3 USIM INTERFACE

TD2115M has a standard USIM interface which support the requirements of 3GPP specification. The USIM interface is powered by USIM_VDD. It is 3.0V or 1.8V typically.

Table 5-3 : USIM Interface

Pin Name	Pin No.	Comment
USIM_VDD	19	Supply power to USIM card. 3.0V or 1.8V power domain, depending on VDDIO. Connect with a TVS diode for ESD protection.
USIM_GND	20	Dedicated ground for USIM card ground.
USIM_CLK	21	USIM clock signal. Connect with a TVS diode for ESD protection.
USIM_DATA	22	USIM data signal. Connect with a TVS diode for ESD protection.
USIM_RST	23	UISM reset signal. Connect with a TVS diode for ESD protection.

The reference design of USIM circuit is shown as below. It is recommended to have the following suggestions.

- Add TVS diodes for ESD protection and place it as close as possible to USIM socket.
- Add 22Ω resistors in series connection between TD2115M and USIM socket for signal integrity.
- Add 22pF capacitors and place it as close as to USIM socket for reducing EMI.
- Add a 20K pull-up resistor for the requirement of USIM.
- Keep USIM socket as far away from any RF trace and VBAT.
- Keep USIM_CLK trace as straight as possible. Use arc-shaped traces instead of right-angle bends. Do not use via for USIM_CLK trace and use ground or guard traces for reducing EMI.

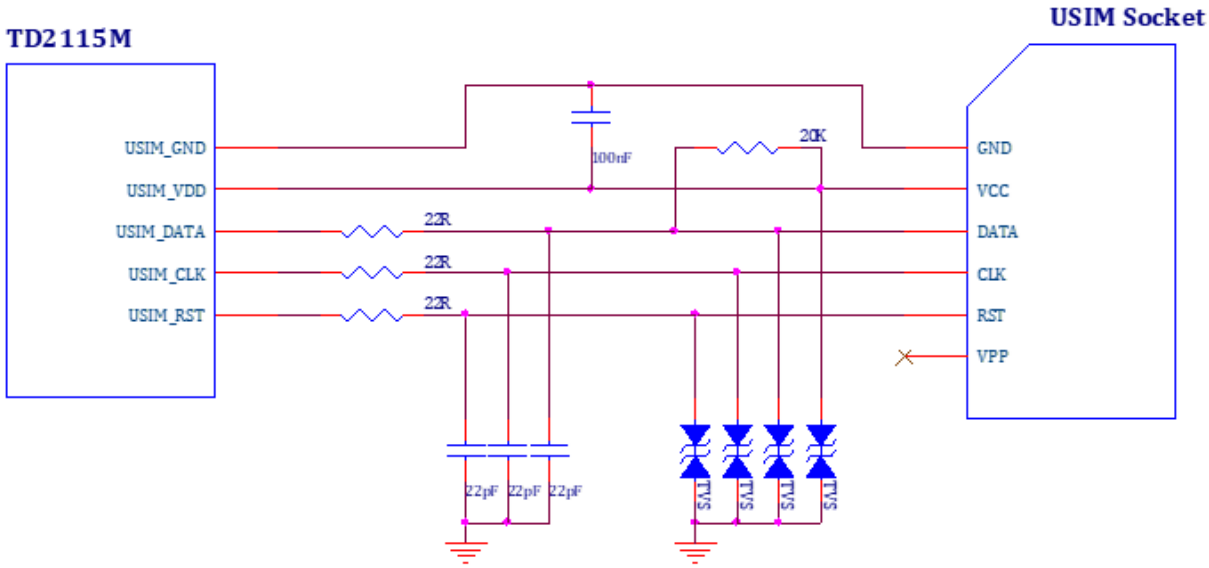

Figure 5-3 : Reference Design of USIM Interface

5.4 ADC/DAC INTERFACE

A 10-bit ADC or a 10-bit DAC is supported by TD2115M via AIO<1:0>. The ADC is available in Active and Standby modes of operation and the DAC is available in all modes of operation.

Table 5-4 : ADC/DAC Interface

Pin Name	Pin No.	Comment
AIO_1	13	Analog input and output. Used for ADC or DAC. Leave it open if not used.
AIO_0	14	Analog input and output. Used for ADC or DAC. Leave it open if not used.

5.5 SPI INTERFACE

TD2115M has a Serial Peripheral Interface (SPI) for supporting the external serial flash.

Table 5-5 : SPI Interface

Pin Name	Pin No.	Comment
SPI_CLK	3	Serial data clock input. Leave it open if not used.
SPI_SI	4	Serial data input. Leave it open if not used.
SPI_CS	5	Chip select. Leave it open if not used.
SPI_SO	6	Serial data output. Leave it open if not used.

The reference design of SPI circuit is shown as below. It is recommended to have the following suggestions.

- A 0.1uF decoupling capacitor is recommended for power supply.

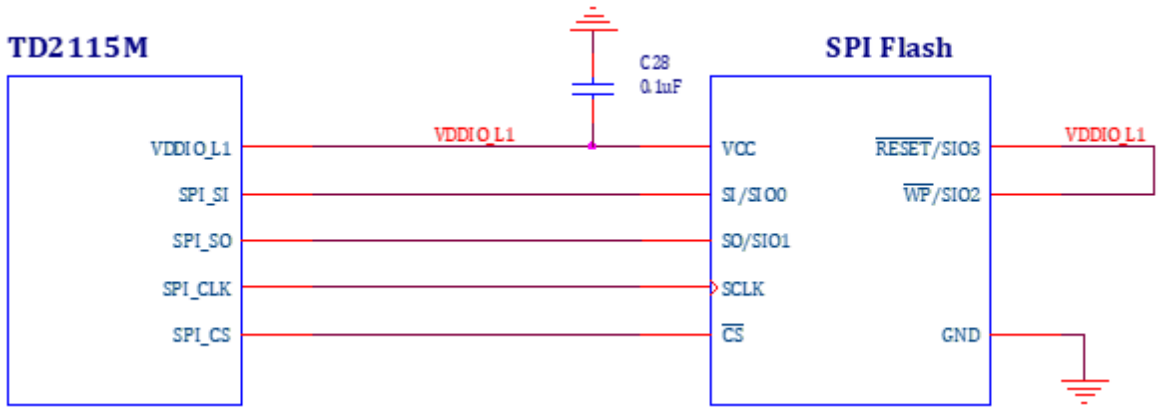

Figure 5-4 : Reference Design of SWD Interface

5.6 NETLIGHT INTERFACE

A NETLIGHT signal is used for the indication of network status.

Table 5-6 : NETLIGHT Interface

Pin Name	Pin No.	Comment
NETLIGHT	37	3.0V power domain. Leave it open if not used.

The following reference design is a LED indication of network status.

- The module is not attached to network when LED is “Light off”.
- The module is attached to network when LED is “Light on”.

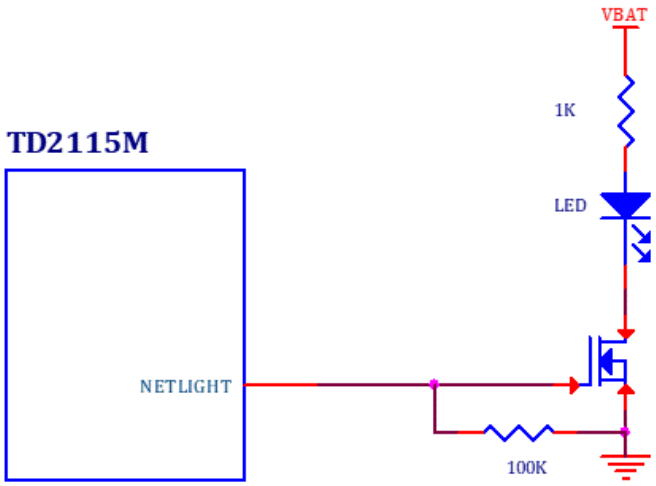

Figure 5-5 : Reference Design of LED Indication

5.7 POWER SUPPLY

TD2115M is powered via VBAT power supply. The VBAT voltage ranges from 3.1 ~ 4.2V with a typical 3.6V operation and is required at least 0.5A current capability.

Table 5-7 : Power Interface

Pin Name	Pin No.	Comment
VBAT	16	Main power supply input. VBAT= 3.1 ~ 4.2V.
VBAT	17	Main power supply input. VBAT= 3.1 ~ 4.2V.

The reference design of Power circuit is shown as below. It is recommended to have the following suggestions.

- A 100uF Tantalum capacitor with low ESR is recommended.
- Place decoupling capacitors as close as possible to VBAT pads from small capacitance to large capacitance.
- Add a TVS diode for ESD protection.
- Keep VBAT trace as wider as possible.

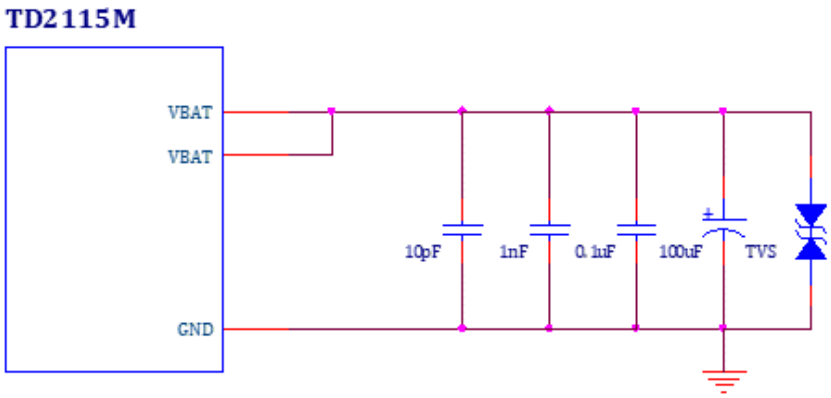

Figure 5-6 : Reference Design of Power Supply

5.8 ANTENNA INTERFACE

A RF_ANT is the antenna port for transmitting and receiving. The 50Ω impedance control of trace route is very important.

Table 5-8 : Antenna Interface

Pin Name	Pin No.	Comment
RF_ANT	47	RF antenna port. The 50Ω impedance control is required.

The reference design of RF antenna circuit is shown as below. It is recommended to have the following suggestions.

- Add a π-type matching circuit for tuning RF performance.
- Add a ESD protection diode with ultra-low capacitance.
- The RF antenna trace must be as short as possible and controlled with a 50Ω impedance. The 50Ω characteristic impedance can be computed with a simulation tool, such as APPCAD.

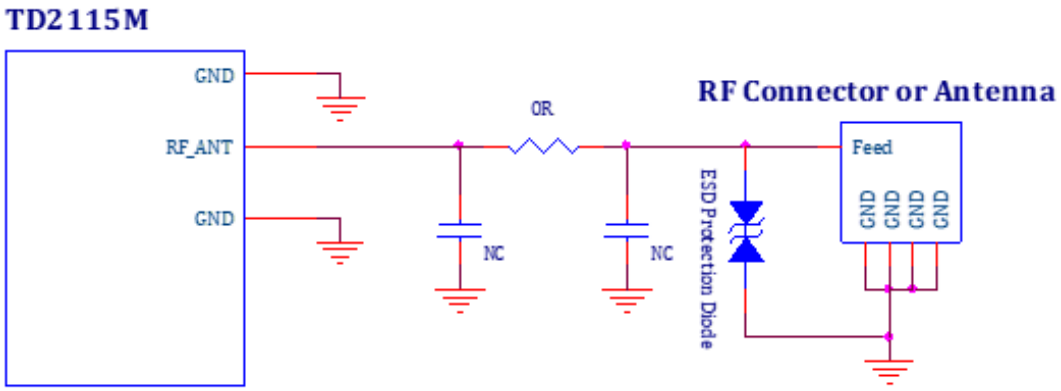

Figure 5-7 : Reference Design of RF Antenna

6 MECHANICAL SPECIFICATIONS

6.1 PHYSICAL DIMENSIONS

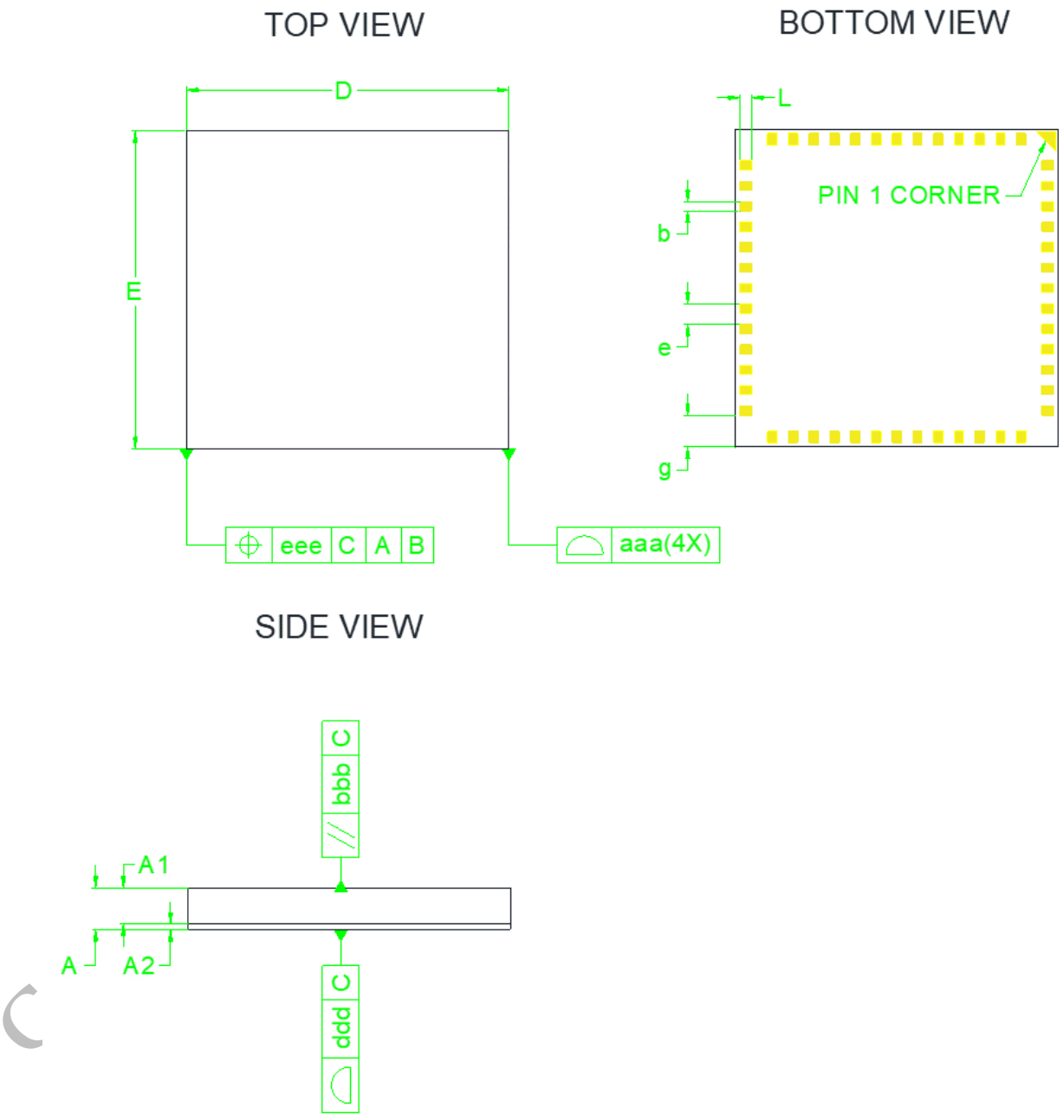

Figure 6-1 : Module Mechanical Outline

Table 6-1 : Dimension of Mechanical Outline

Symbol	Dimension (mm)		
	Min.	Typ.	Max.
A	1.80	1.85	1.90
A1		1.60	

A2		0.25	
b	0.35	0.40	0.45
D	13.90	14.00	14.10
E	13.90	14.00	14.10
e		0.90	
L	0.45	0.50	0.55
g		1.40	
aaa		0.10	
bbb		0.10	
ddd		0.10	
eee		0.10	

6.2 MARKING INFORMATION

Figure 6-2 : TD2115M Markings

Table 6-2 : TD2115M Markings

Marking	Description
TD2115M	Model name
TD2115M-HLB-01	Hardware version
1818NT	Date code and manufacturer code
R03	Product identification

7 REFERENCE PCB DESIGN

7.1 PCB LAND PATTERN DESIGN

Unit: mm

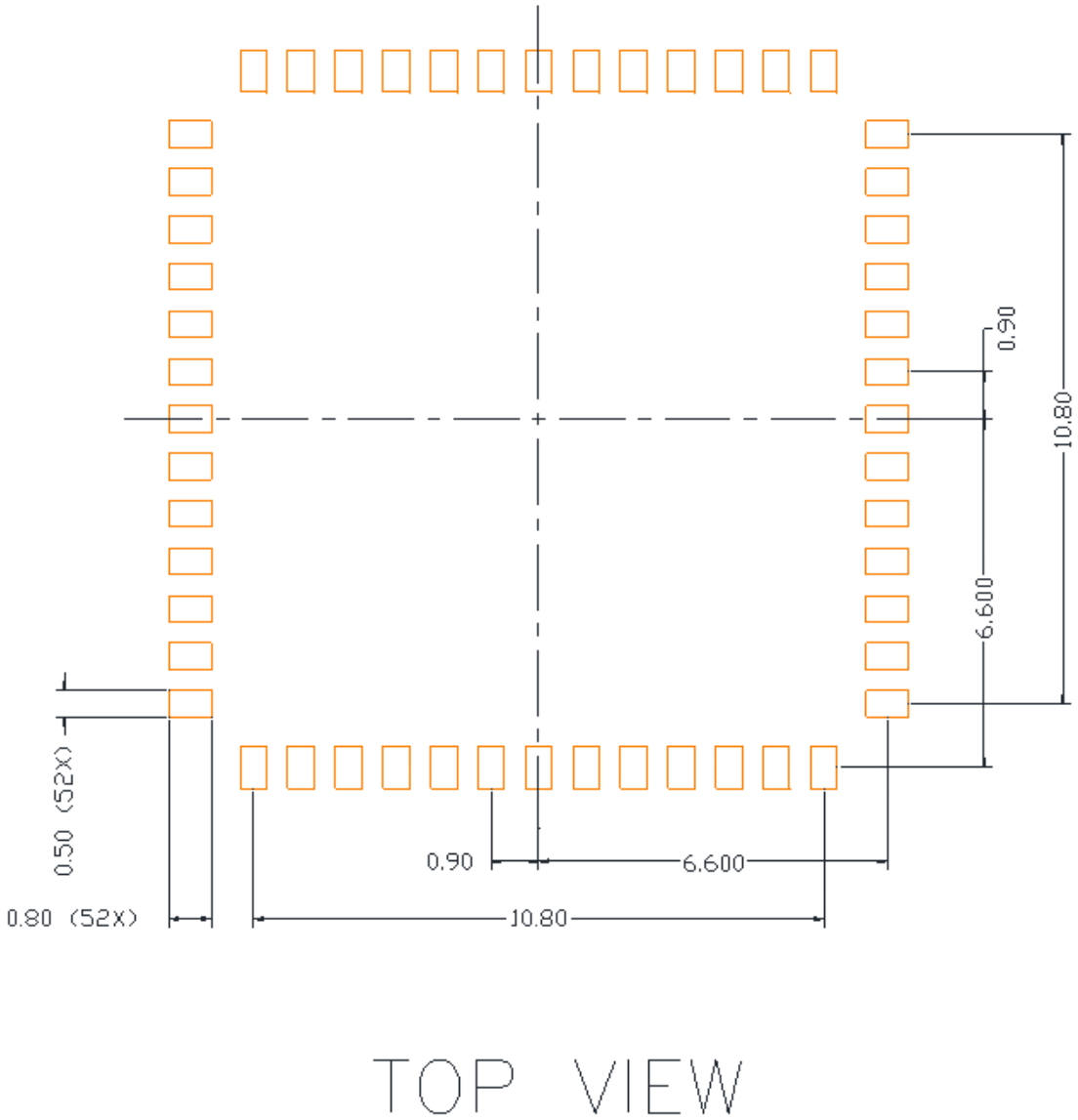

Figure 7-1 : Recommended PCB Land Design

7.2 SOLDER MASK DESIGN

Unit: mm

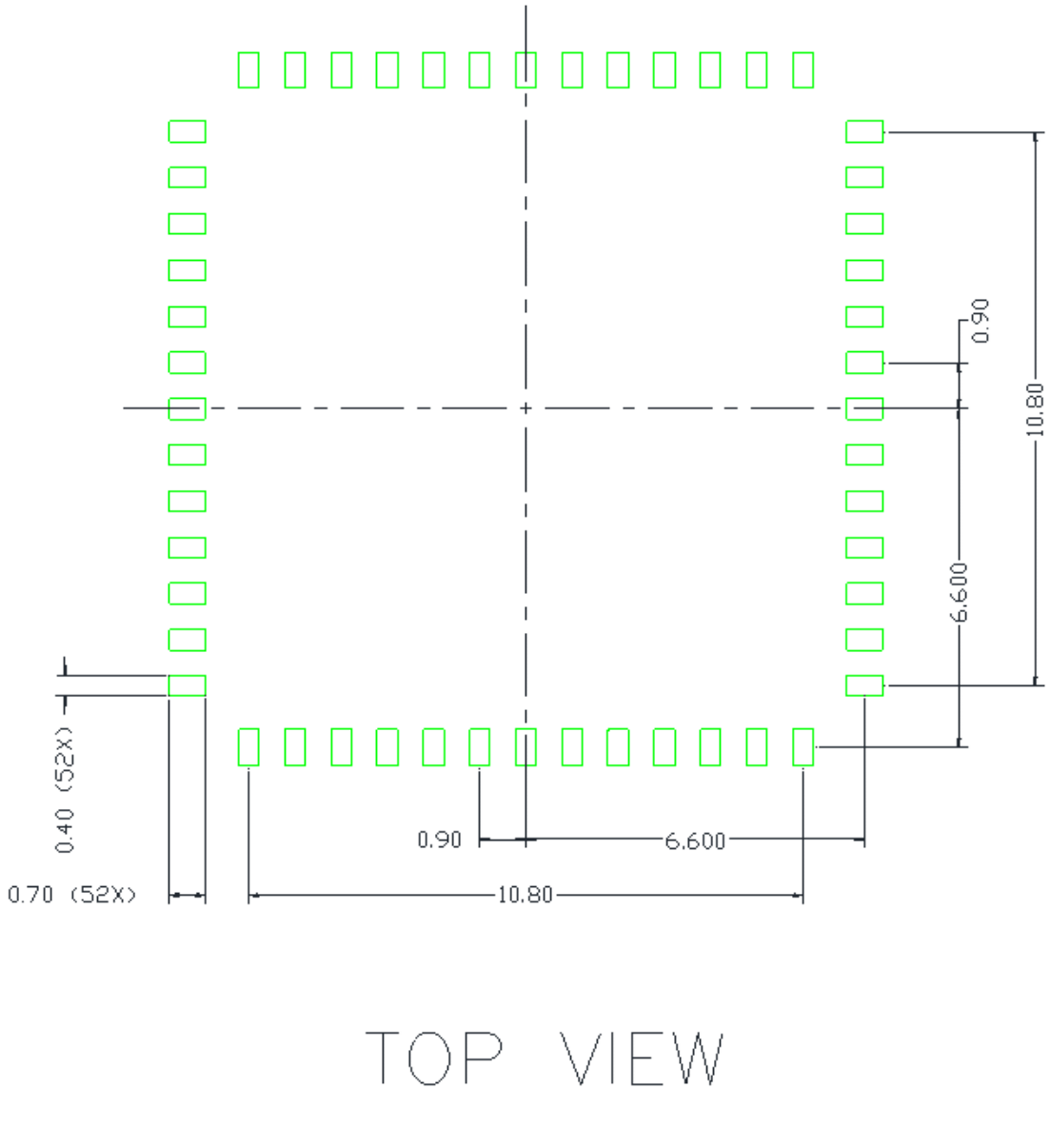

Figure 7-2 : Recommended Solder Mask Design

8 RECOMMENDED REFLOW PROFILE

8.1 REFLOW PROFILE

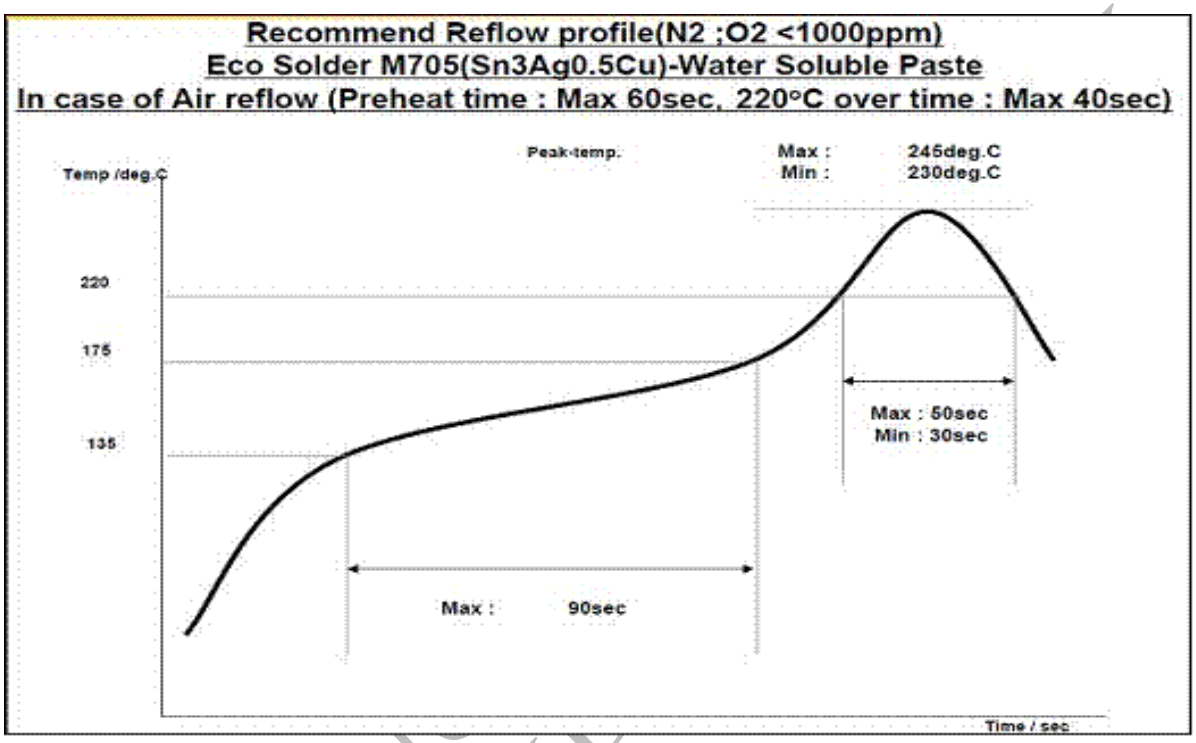

Figure 8-1 : Reflow Profile

Table 8-1 : Temperature Value for Reflow Profile

Parameter	Value
Preheat Ramp-up Rate	125°C to 217°C < 1°C /sec
Time at T > 217°C	60 sec to 90 sec
Peak Temperature	245°C
Cooling Ramp-down Rate	< 1°C / sec
Time From 25°C to peak	240 to 360 sec

Note 1: The peak temperature of reflow profile should be less than 250°C.
Note 2: If the PCB is required double-sided soldering, it is strongly suggested that the module is mounted at the second side of PCB after completing soldering profile for the first side of PCB.

8.2 REWORK GUIDELINE

Reference guideline was listed below for de-mount process from PCB.

- PCBA should be baked for 24 hours at 125°C.
- De-mount TD2115M module from PCB with hot air gun. Heat air should be less than 380 °C, 30 seconds.

9 PACKING INFORMATION

9.1 REEL TAPE PACKING

TBD

9.2 LABEL DEFINITION

TBD

9.3 PACKING METHOD

TBD

10 HANDLING MOISTURE SENSITIVITY

10.1 MOISTURE SENSITIVITY LEVEL

Follow the latest IPC/JEDEC J-STD-020 standard revision for moisture sensitivity qualification. TD2115M module is classified as MSL3.

Table 10-1 : Moisture Sensitivity Level

Moisture Sensitivity Level	Condition	Floor Life
1	≦30℃ and 85%RH	Unlimited
2	≦30℃ and 60%RH	1 year
3	≦30℃ and 60%RH	168 hours
4	≦30℃ and 60%RH	72 hours
5	≦30℃ and 60%RH	48 hours
6	≦30℃ and 60%RH	6 hours

10.2 STORAGE CONDITION

TD2115M, as delivered in tape-and-reel carrier, must be stored in a vacuum-sealed bag. Shelf life is 12 months. This is required an ambient temperature less than 40 ^{0}C and relative humidity less than 90%.

10.3 OUT-OF-BANG DURATION

TD2115M module can be exposed for 168 hours to an environment with a maximum temperature of 30^{0}C and a maximum relative humidity of 60%.

10.4 BAKING REQUIREMENT

After bag is opened, module that will be subjected to reflow solder or other high temperature process must be

- Mounted within: 168 hours of factory condition ≦30^{0}C/60%RH,
- Stored at ≦ 30^{0}C/10%RH.

Module require bake before mounting, if Humidity Indicator Card reads ＞10% when read at 23±5^{0}C. If baking is required, following baking condition should be used.

- 24 hours at 125 ±5^{0}C .