

# PRODUCT SPECIFICATION

<b>Product Name</b>	<b>AI50H</b> LoRa Wireless Communication Module
<b>Version</b>	<b>C</b>
<b>Doc No</b>	<b>901-13401</b>
<b>Date</b>	<b>2021/12/22</b>



## Document History

Date	Revised Contents	Revised By	Version
2021/06/21	Initial release	Jack	A
2021/10/21	Recommended Footprint	Jack	B
2021/12/22	Sigfox Ready (RC1) Spec. Product Making and Regulation	Jack	C

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## 1. General Description

The AI50H integrates ARM Cortex®-M4 (32-bit RISC core operating at a frequency of up to 48 MHz) MCU with LoRa/Sigfox modulation that provides ultra-long range spread spectrum communication and high interference immunity whilst minimizing current consumption.

The AI50H can achieve a sensitivity of over -136 dBm. The high sensitivity combined with the integrated +21 dBm (LoRa), +13dBm (fixed for Sigfox RC1) power amplifier yields industry leading link budget making it optimal for any low data rate application requiring range or robustness. LoRa also provides significant advantages in both blocking and selectivity over conventional modulation techniques, solving the traditional design compromise between range, interference immunity and energy consumption.

### ➤ Feature:

- Chipset: STM32WLE5(single core)
- High performance ARM® Cortex®-M4 32-bit RISC core operating up to 48 MHz frequency
- Embedded memories (256 Kbytes of Flash memory and 64 Kbytes of RAM)
- Hardware encryption AES 256-bit
- True random number generator (RNG)
- CRC calculation unit
- Unique device identifier (64-bit UID compliant with IEEE 802-2001 standard)
- 96-bit unique die identifier
- Hardware public key accelerator (PKA)
- 32 MHz TCXO & 32 KHz XTAL
- 2 DMA, 2 USART, 1 LPUART, 2 SPI, 3 I2C
- RTC wakeup counter, SysTick, Watchdog
- Modulation: LoRa®, (G)FSK, (G)MSK and BPSK. Sigfox:DBPSK, 2GFSK.
- LoRa:+21 dBm Max. RF output , Sigfox RC1 : +13dBm Max. RF output.
- Programmable bit rate up to 300 kbps
- High sensitivity: down to -138 dBm for LoRa @125kHz, SF12
- Automatic RF Sense and CAD with ultra-fast AFC
- I-PEX MHF Connector
- Small footprint : 20 mm x 20 mm x 1.95 mm(Typ.)
- High-efficiency SMPS step-down converter and independent power supplies for ADC, DAC and comparator analog inputs.
- VBAT mode with RTC and 20x32-byte backup registers, battery voltage monitoring



## 1-1. Block Diagram

A simplified block diagram of the AI50H module is depicted as figure 1 below.

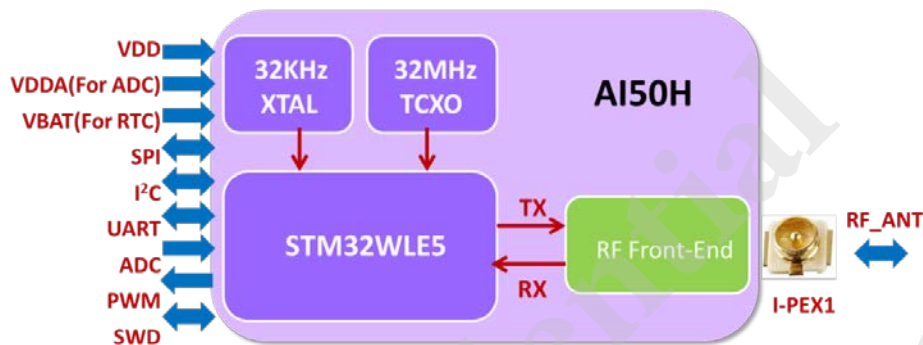


Figure 1, Block Diagram

## 1-2. Product Version

Part Number	Frequency Range	Spreading Factor	Bandwidth (KHz)	Effective Bitrate (bps)	Est. Sensitivity ( dBm )
AI50H	863 – 930 MHz	5 - 12	7.8 - 500	LoRa BR : 0.013 – 17.4 kb/s (G)FSK BR : 0.6 - 300 kb/s	-138 @125kHz, SF12

## 1-3. Specification

Model Name	AI50H
Product Description	LoRa Wireless Communication Module
Host Interface	UART
<b>Operation Conditions</b>	
Temperature	<ul style="list-style-type: none"> <li>■ Storage : -50°C ~ +125°C</li> <li>■ Operating : -40°C ~ +85°C</li> <li>■ Low Power Dissipation : -40°C ~ +95°C (*Note)</li> </ul>
Humidity	<ul style="list-style-type: none"> <li>■ Operating : 10 ~ 95% (Non-Condensing)</li> <li>■ Storage : 5 ~ 95% (Non-Condensing)</li> </ul>
RF Output	I-PEX MHF Connector
Dimension	20 mm x 20 mm x 1.95 mm(Typ.)
Package	LGA 58Pin – Stamp hole type

\*Note: Low Power Dissipation: means low TX duty cycle and low GPIO driving and sinking current

## 2. Electrical Characteristics

### 2-1. Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Standard operating voltage	-0.3		3.9	V
V <sub>IN</sub>	Input voltage on digital pins	-0.3		3.9	V
P <sub>mr</sub>	RF Input Level			+10	dBm

### 2-2. Recommended Operating Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Standard operating voltage		1.8	3.3	3.6	
VDDA	Analog supply voltage	ADC or COMP used	1.71		3.6	V
		VREFBUF used	2.4			
		ADC, COMP, REFBUF not used	0			
VBAT	Backup operating voltage		1.55		3.6	
VREF+	Positive reference voltage	VDDA ≥ 2 V	2		VDDA	
		VDDA < 2 V	VDDA			
ML	RF Input Level				+10	dBm

## 2-3. Power Consumption Characteristics

### 2-3-1. AI50H Power supply scheme

The devices embed two different regulators: one LDO and one DC/DC (SMPS). The SMPS can be optionally switched-on by software to improve the power efficiency. As LDO and SMPS operate in parallel, the SMPS switch-on is transparent to the user and only the power efficiency is affected.

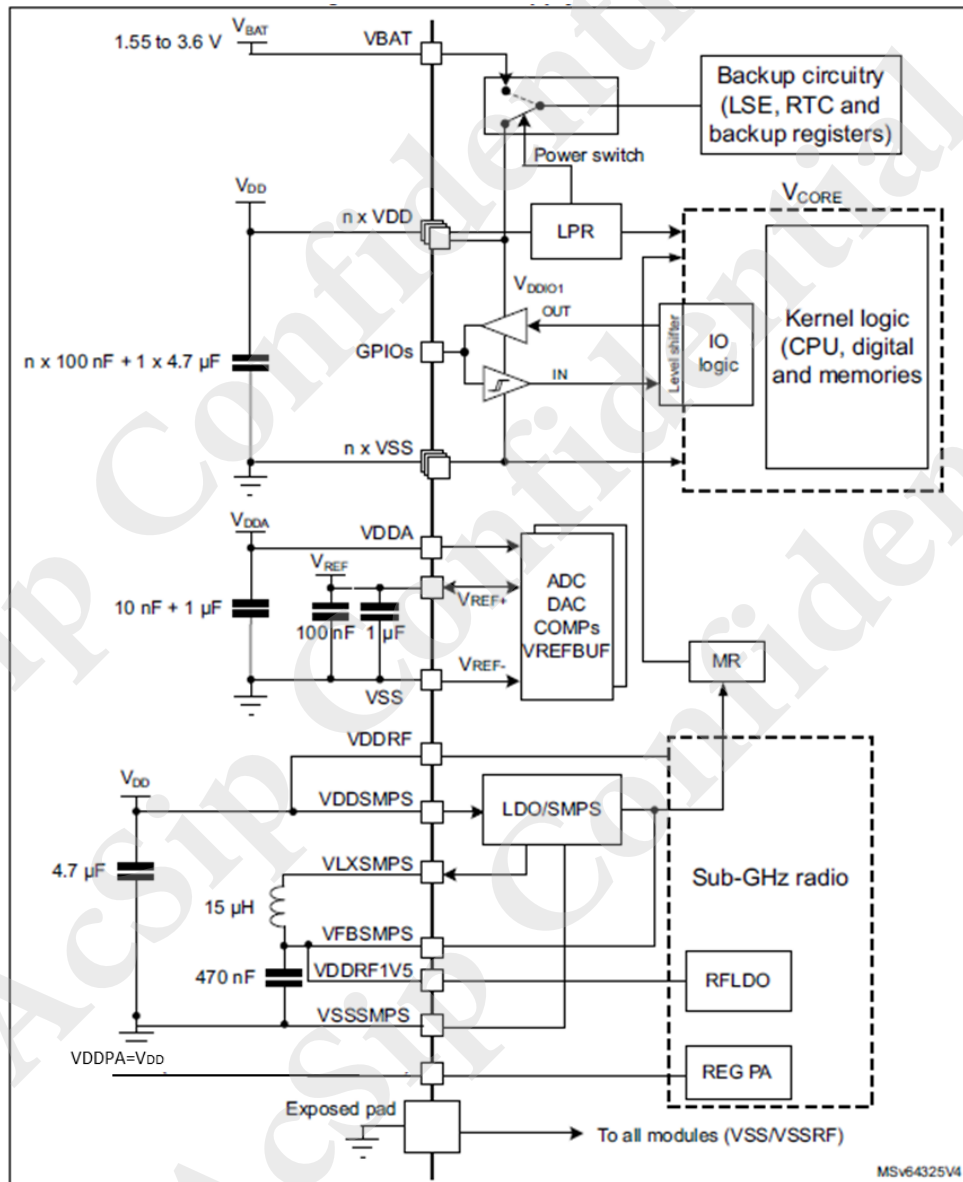


Figure 2, AI50H Power supply scheme





## 2-3-2. Current consumption measurement scheme

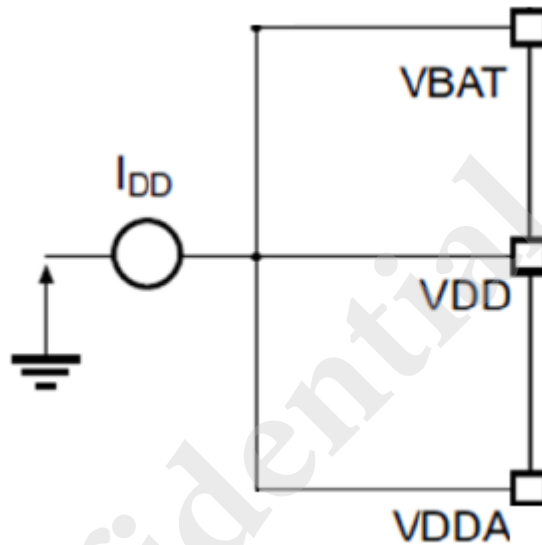


Figure 3, Current consumption measurement scheme

## 2-3-3. The current consumption

VDD = 3.3 V. The current consumption is measured as described in *Figure 3*.  $I_{DD}$  includes current consumption of all supplies (VDD, VDDA, and VBAT).

Symbol	Parameter	Conditions	Typ.	Max	Unit
$I_{DDSL}$	Supply current in Sleep mode(Stop 2)		1.3		$\mu A$
$I_{DDR}$	Supply current in Receive mode(SMPS mode used) (SMPS 40 mA max)	RX boosted, LoRa 125 KHz	6.5		mA
$I_{DDT}$	Supply current in transmit mode with impedance matching(SMPS on) (SMPS 40 mA max) 863~930MHz	RF SetPW = 22dBm RF SetPW = 20dBm RF SetPW = 18dBm RF SetPW = 16 dBm	128 118 108 100		mA

## 2-4. RF Characteristics

### 2-4-1. Electrical Specifications

The table below gives the electrical specifications for the transceiver operating with LoRa modulation. Following conditions apply unless otherwise specified:

- VDD = 3.3 V
- Temperature = 25 °C
- FRF = 863 / 915 MHz
- RF impedances matched
- Transmit mode output power defined into a 50 ohm load impedance
- FSK BER = 0.1%, 2-level FSK modulation without pre-filtering, BR = 4.8 kb/s, FDA = ± 5 kHz, BW\_F = 20 kHz double-sided
- LoRa® PER = 1%, packet 64 bytes, preamble 8 symbols, CR = 4/5, CRC on payload enabled

### 2-4-2. Receive Mode Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
RXS_2FB	Sensitivity 2-FSK, RX boosted gain, split RF paths for RX and Tx, RF switch insertion loss excluded	BR=0.6Kbit/s, FDA=0.8 kHz, BW=4 kHz	-	-125	-	dBm
		BR=1.2Kbit/s, FDA=5 kHz, BW=20 kHz	-	-123	-	
		BR=4.8Kbit/s, FDA=5 kHz, BW=20 kHz	-	-117	-	
		BR=38.4bit/s, FDA=40kHz, BW=160 kHz	-	-108	-	
		BR=250Kbit/s, FDA=125kHz, BW=500 kHz	-	-103	-	
RXS_LB	Sensitivity LoRa, RX boosted gain, split RF paths for RX and Tx, RF switch insertion loss excluded	BW = 10.4 kHz, SF = 7	-	-135	-	dBm
		BW = 10.4 kHz, SF = 12	-	-148	-	
		BW = 125 kHz, SF = 7	-	-125	-	
		BW = 125 kHz, SF = 12	-	-138	-	
		BW = 250 kHz, SF = 7	-	-122	-	
		BW = 250 kHz, SF = 12	-	-135	-	
		BW = 500 kHz, SF = 7	-	-118	-	
		BW = 500 kHz, SF = 12	-	-130	-	
RXS_2F	Sensitivity 2-FSK, RX power saving gain with direct tie connection between RX and Tx	BR=4.8 Kbit/s, FDA=5 kHz, BW=20 kHz	-	-115	-	



RXS_L	Sensitivity LoRa, RX power saving gain with direct tie connection between RX and Tx	BW = 125 kHz, SF = 12	-	-135	-	
CCR_F	Co-channel rejection, FSK	-	-	-9	-	dB
CCR_L	Co-channel rejection, LoRa	SF = 7	-	7	-	
		SF = 12	-	19	-	
ACR_F	Adjacent channel rejection, FSK	Offset = $\pm 50$ kHz	-	44	-	
ACR_L	Adjacent channel rejection, LoRa	Offset = $\pm 1.5 \times BW\_L$ , BW = 125 kHz, SF = 7	-	60	-	
		Offset = $\pm 1.5 \times BW\_L$ , BW = 125 kHz, SF = 12	-	71	-	
BI_F	Blocking immunity, FSK	Offset = $\pm 1$ MHz, BR = 4.8 Kbit/s, FDA = 5 kHz, BW = 20 kHz	-	67	-	
		Offset = $\pm 2$ MHz, BR = 4.8 Kbit/s, FDA = 5 kHz, BW = 20 kHz	-	70	-	
		Offset = $\pm 10$ MHz, BR = 4.8 Kbit/s, FDA = 5 kHz, BW = 20 kHz	-	76	-	
BI_L	Blocking immunity, LoRa	Offset = $\pm 1$ MHz, BW = 125 kHz, SF = 12	-	87	-	dB
		Offset = $\pm 2$ MHz, BW = 125 kHz, SF = 12	-	91	-	
		Offset = $\pm 10$ MHz, BW = 125 kHz, SF = 12	-	96	-	
IIP3	Third order input intercept point	Unwanted tones are 1 MHz and 1.96 MHz above LO. 868 to 915 MHz band	-	-9	-	dBm
IMA	Image attenuation	Without IQ calibration	-	30	-	dB
		With IQ calibration	-	54	-	
BW_F	DSB channel filter BW, FSK	Programmable, typical values	4.8	-	467	kHz
TS_RX	Receiver wakeup time	FS to RWX	-	41	-	$\mu$ s
FERR_L	Maximum tolerated frequency offset between transmitter and receiver, SF7 to SF12	All bandwidths, $\pm 25$ % of BW. The tighter limit between this line and the three lines below applies.	-	$\pm 25$	-	BW
		SF12	-50	-	50	ppm
		SF11	-100	-	100	
	Maximum tolerated frequency offset between transmitter and receiver, SF10 to SF12	SF10	-200	-	200	

## 2-4-3. Transmit Mode Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
TXOP	Maximum RF output power Highest power step setting	LoRa	20	21	22	dBm
		Sigfox, RC1		13 <sup>(1)</sup>		dBm
TXDRP	RF output power drop versus supply voltage	RF SetPW =22dBm +21 dBm, VDD = 2.7 V +21 dBm, VDD = 2.4 V +21 dBm, VDD = 1.8 V		2 3 6		dB
TXPRNG	RF output power range	Programmable in 31 step typical value	TXOP-31		TXOP	dBm
TXACC	RF output power step accuracy			± 2		dB
TXRMP	Power amplifier ramping time	Programmable	10	-	3400	µs
TS_TX	Tx wake-up time	Frequency Synthesizer enabled		36 + PA ramping		µs

(1) The RF power can not be modified for Sigfox RC1

## 2-4-4. Digital I/O Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	Input High Voltage		0.7*VDD		VDD+0.3	V
V <sub>IL</sub>	Input Low Voltage		-0.3		0.3*VDD	V
V <sub>IL-N</sub>	Input Low Voltage for pin NRESET		-0.3		0.2*VDD	V
V <sub>OH</sub>	Output High Voltage	I <sub>max</sub> = -2.5 mA	0.9*VDD		VDD	V
V <sub>OL</sub>	Digital output level low	I <sub>max</sub> = 2.5 mA	0		0.1*VDD	V
I <sub>leak</sub>	Digital input leakage current (NSS, MOSI, SCK)				1	µA

## 3. Pin Definition

### 3-1. Pin Definition

Pin	New	Definition	I/O	Description
1	PA13	PA13	I/O	MCU pin name: PA13
2	PA14	PA14	I/O	MCU pin name: PA14
3	GND	GND	—	Ground pin
4	VBAT	VBAT	I	VDD (FOR RTC Power)
5	PC13	PC13	I/O	MCU pin name: PC13
6	VREF+	VREF+	I	Input reference voltage for ADC
7	VDDA	VDDA	I	External analog power supply for A/D Converters
8	PA15	PA15	I/O	MCU pin name: PA15
9	PB15	PB15	I/O	MCU pin name: PB15
10	PB3	PB3	I/O	MCU pin name: PB3
11	PB4	PB4	I/O	MCU pin name: PB4
12	PB5	PB5	I/O	MCU pin name: PB5
13	PB6	PB6	I/O	MCU pin name: PB6
14	GND	GND	—	Ground pin
15	PB7	PB7	I/O	MCU pin name: PB7
16	GND	GND	—	Ground pin
17	PB8	PB8	I/O	MCU pin name: PB8
18	PB9	PB9	I/O	MCU pin name: PB9
19	PC0	PC0	I/O	MCU pin name: PC0
20	PC1	PC1	I/O	MCU pin name: PC1
21	PC2	PC2	I/O	MCU pin name: PC2
22	PC3	PC3	I/O	MCU pin name: PC3
23	PC4	PC4	I/O	MCU pin name: PC4
24	PC5	PC5	I/O	MCU pin name: PC5
25	PC6	PC6	I/O	MCU pin name: PC6
26	GND	GND	—	Ground pin
27	GND	GND	—	Ground pin
28	GND	GND	—	Ground pin
29	GND	GND	—	Ground pin
30	GND	GND	—	Ground pin

31	NC	—	—	—
32	GND	GND	—	Ground pin
33	PA2	PA2	I/O	MCU pin name: PA2
34	PA3	PA3	I/O	MCU pin name: PA3
35	PA4	PA4	I/O	MCU pin name: PA4
36	PA5	PA5	I/O	MCU pin name: PA5
37	PA6	PA6	I/O	MCU pin name: PA6
38	PA7	PA7	I/O	MCU pin name: PA7
39	GND	GND	—	Ground pin
40	GND	GND	—	Ground pin
41	Boot 0	Boot 0	I	Boot mode selection pin
42	NRST	NRST	I	Hardware reset pin
43	PB11	PB11	I/O	MCU pin name: PB11
44	PB10	PB10	I/O	MCU pin name: PB10
45	PA9	PA9	I/O	MCU pin name: PA9
46	PA8	PA8	I/O	MCU pin name: PA8
47	VDD	VDD	I	VDD
48	GND	GND	—	Ground pin
49	PB1	PB1	I/O	MCU pin name: PB1
50	PB2	PB2	I/O	MCU pin name: PB2
51	PB12	PB12	I/O	MCU pin name: PB12
52	PB13	PB13	I/O	MCU pin name: PB13
53	PB14	PB14	I/O	MCU pin name: PB14
54	PA10	PA10	I/O	MCU pin name: PA10
55	PA11	PA11	I/O	MCU pin name: PA11
56	PA12	PA12	I/O	MCU pin name: PA12
57-58	GND	GND	—	Ground pin

### 3-2. Pin Assignment

The module will conform to the following pin map (top view):

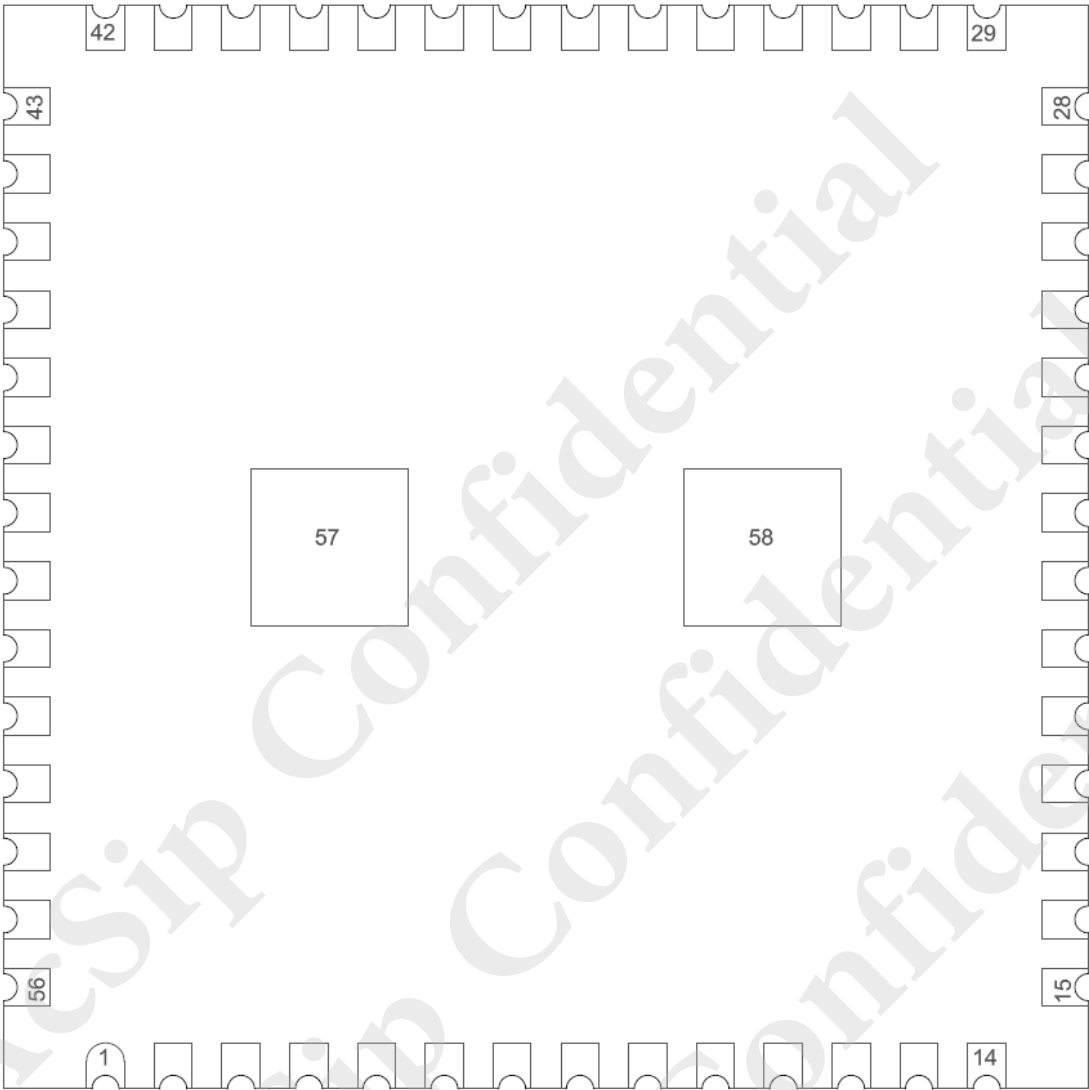


Figure 4, Pin Assignment



### 3-3. Mechanical Dimension (Typ.)

Unit: mm

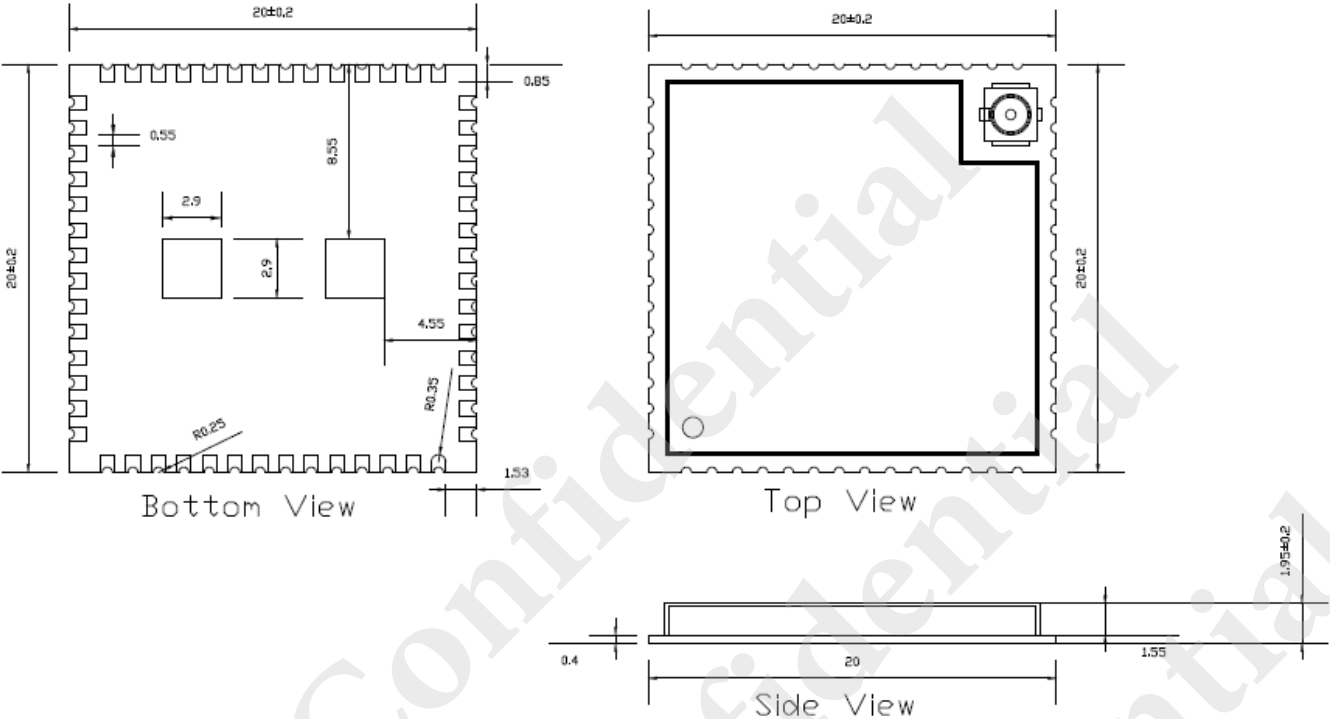


Figure 5, Mechanical Dimension (Typ.)





## 4. Recommended Footprint

Unit: mm

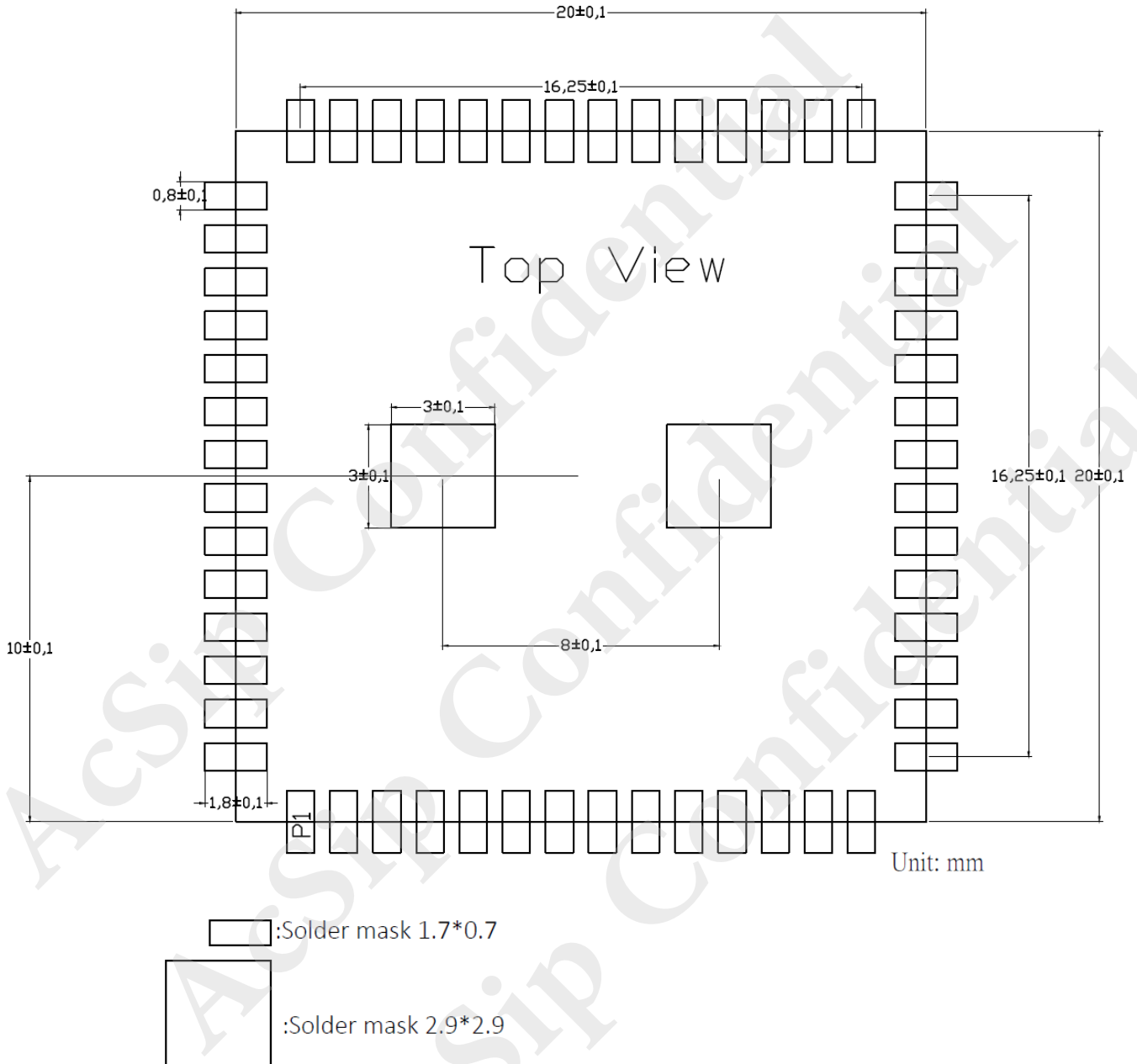
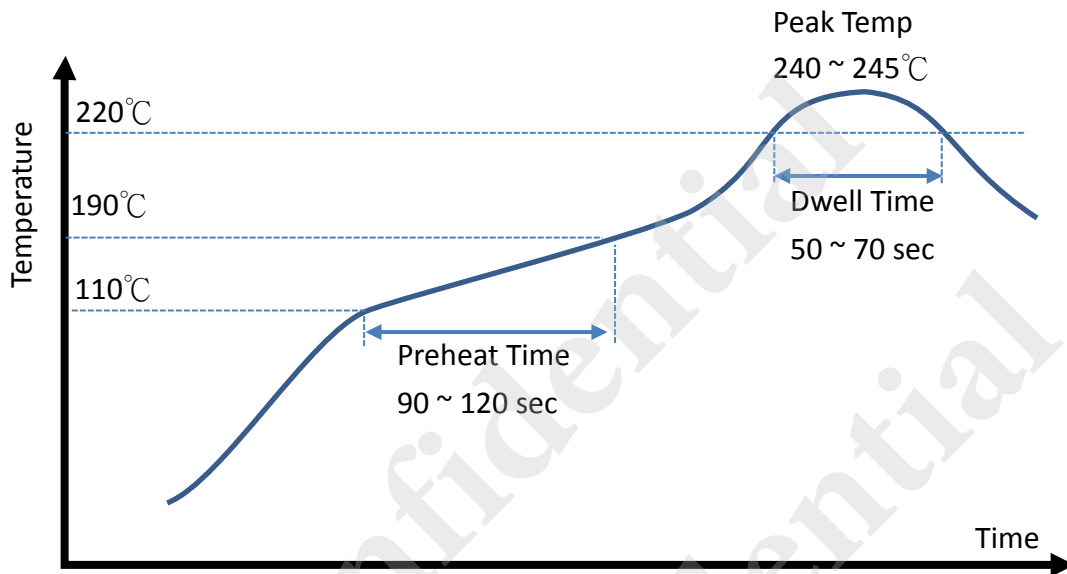


Figure 6, Recommended Footprint



## 5. Recommended Reflow Profile



Preheat time	110 ~ 190 °C : 90 ~ 120 sec
Dwell time	above 220 °C : 50 ~ 70 sec
Peak Temp	240 ~ 245 °C
Ramp Up/Down Rate	Up : 1~3 °C/sec Down: 1~5 °C/sec

The recommended reflow profile is provided as a guideline. Optimal profile may differ due to oven type, assembly layout or other process variables. Nitrogen atmosphere is strongly recommended for best soldering result.

Figure 7, Recommended Reflow Profile



## 6. Module Preparation

### 6-1. Handling

Handling the module must wear the anti-static wrist strap to avoid ESD damage. After each module is aligned and tested, it should be transport and storage with anti -static tray and packing. This protective package must be remained in suitable environment until the module is assembled and soldered onto the main board.

### 6-2. SMT Preparation

# Calculated shelf life in sealed bag: 6 months at <math>40^{\circ}\text{C}</math> and <math>90\%</math> relative humidity (RH).

# Peak package body temperature:  $250^{\circ}\text{C}$ .

# After bag was opened, devices that will be subjected to reflow solder or other high temperature process must.

A. Mounted within: 168 hours of factory conditions <math>30^{\circ}\text{C}</math> / <math>60\%</math>RH.

B. Stored at  $\leq 10\%</math>RH with N2 flow box.$

# Devices require baking, before mounting, if:

A. Package bag does not keep in vacuumed while first time open.

B. Humidity Indicator Card is >10% when read at  $23\pm 5^{\circ}\text{C}$ .

C. Expose at 3A condition over 8 hours or Expose at 3B condition over 24 hours.

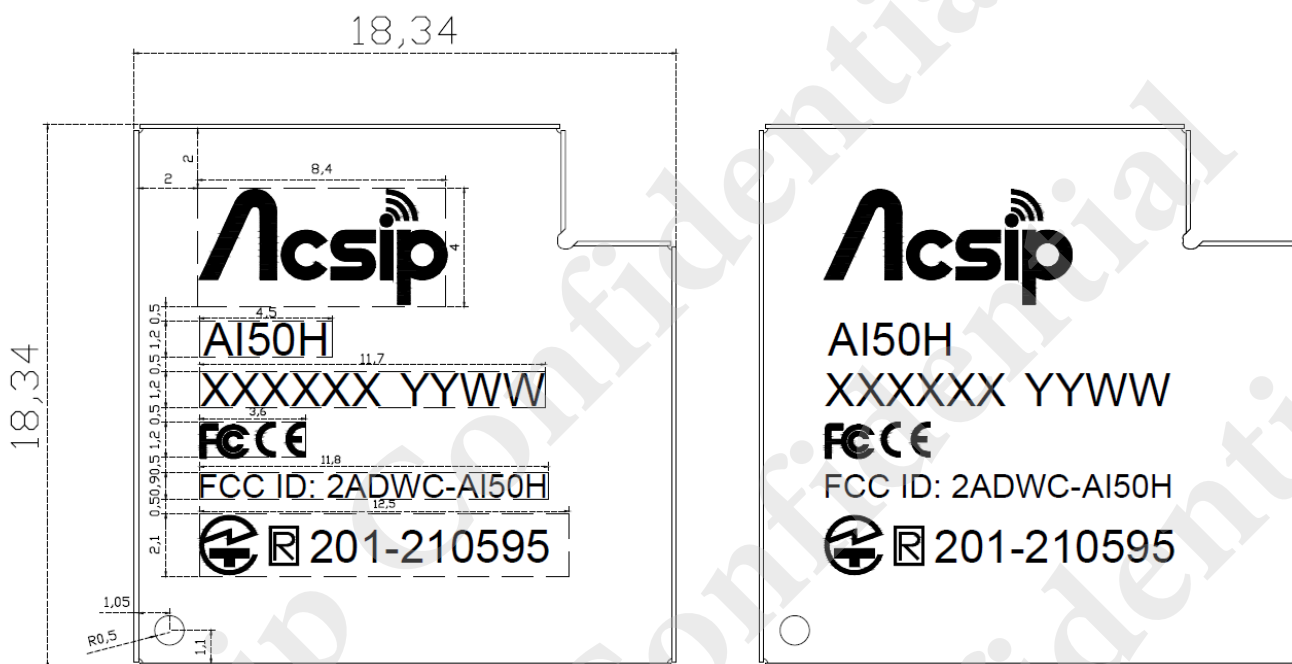
# If baking is required, devices may be baked for 12 hours at  $125\pm 5^{\circ}\text{C}$ .

## 7. Package Information

### 7-1. Product Making

Below is the details standard product marking for AI50H.

Cross reference to the applicable line number and table for a full detail of all the variables.



材質：C7521H-預鍍鎳

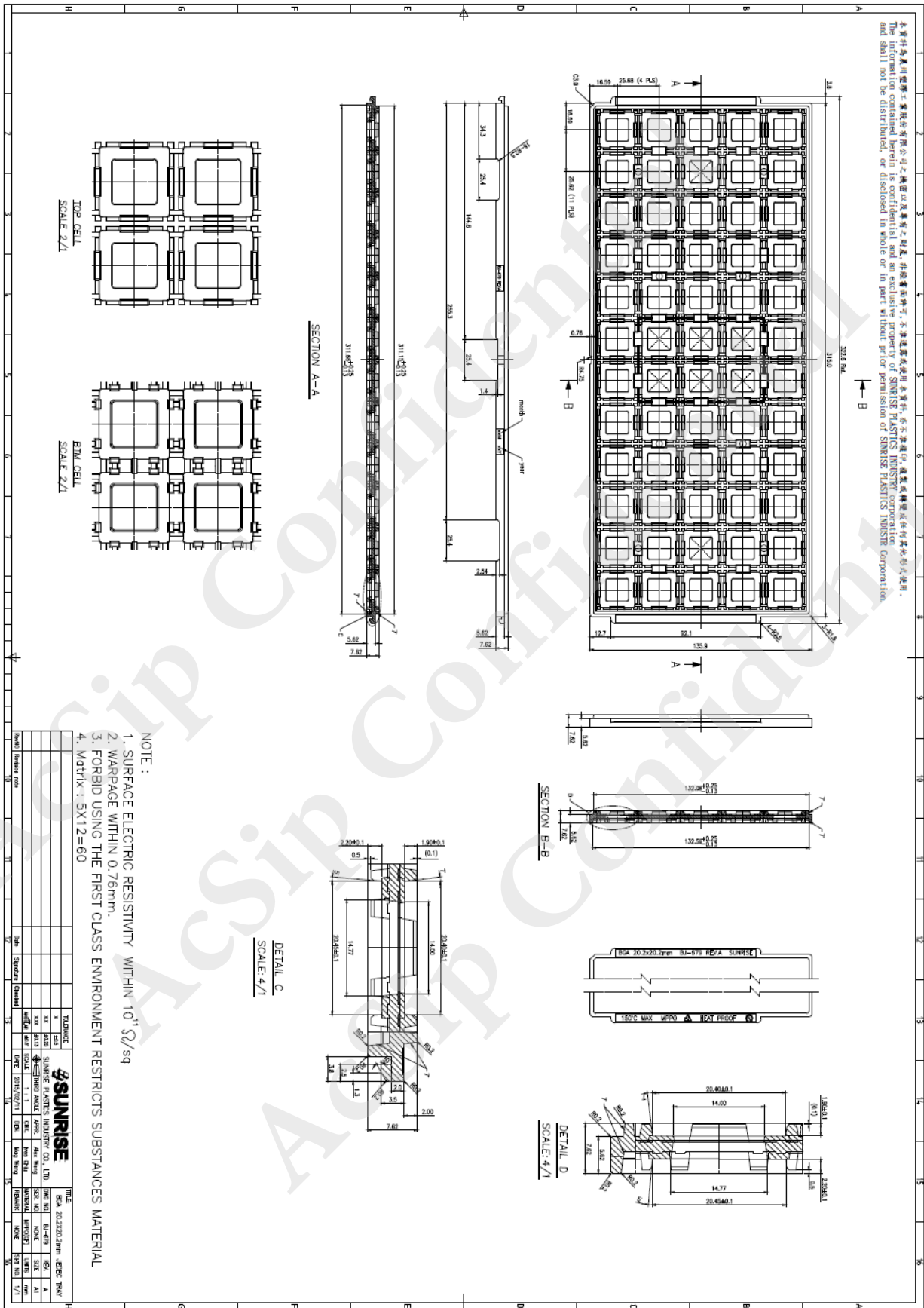
Figure 8, Product Making

### 7-2. Regulation

AI50H has passed to comply with following standards:

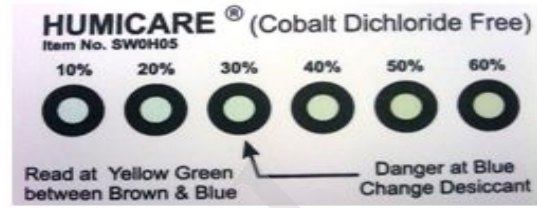
- FCC IDENTIFIER : 2ADWC-AI50H
- CE RED : EN300220, EN301489-1-3, EN62368-1 & EN62311
- TELEC: R 201-210595
- NCC : CCAF21Y10190T1

### 7-3. Tray Dimension





## 7-5. Humidity Indicator Card



Dry

Wet

Indicates 指示點:

10%,20%,30,40%,50%,60% relative humidity

10%,20%,30,40%,50%,60% 相對濕度

Color Change 顏色變化:

Brown (Dry) ---> Blue (Wet)

棕色 (乾燥) ---> 藍色 (潮溼)