# WT41u

DATA SHEET

Wednesday, 25 October 2017 Version 1.1

SILICON LABS

## VERSION HISTORY

| Version | Comment |
|---------|---------|
| 0.8 | First version |
| 0.8.1 | Table reformatting, value updates etc |
| 0.8.2 | Replaced "Bluecore4" with "chipset", added ordering codes |
| 0.8.3 | Rest of table reformatting, added antenna & connector dimension drawings |
| 0.8.4 | Added current consumption, RF characteristics |
| 0.8.5 | Added certification texts |
| 0.8.6 | Added current consumption results, edit TX power variation over VDD range. |
| 0.8.7 | Slight edits to specifications |
| 0.8.8 | OPN descriptions updated |
| 0.8.9 | Bluetooth QDID and Declaration IDs updated |

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# WT41u *Bluetooth®* Module

## DESCRIPTION

WT41u is a long range class 1, Bluetooth® 2.1 + EDR module. WT41u is a highly integrated and sophisticated Bluetooth® module, containing all the necessary elements from Bluetooth® radio and a fully implemented protocol stack. Therefore, WT41u provides an ideal solution for developers who want to integrate Bluetooth® wireless technology into their design with limited knowledge of Bluetooth® and RF technologies. WT41u is optimized for long range applications is available with an integrated chip antenna, an RF pin for a custom on-board antenna or a U.FL connector for an external 2dBi dipole antenna.

By default, WT41u module is equipped with powerful and easy-to-use iWRAP firmware. iWRAP enables users to access Bluetooth® functionality with simple ASCII commands delivered to the module over serial interface - it's just like a Bluetooth® modem.

### APPLICATIONS:

- Hand held terminals
- Industrial devices
- Point-of-Sale systems
- PCs
- Personal Digital Assistants (PDAs)
- Computer Accessories
- Access Points
- Automotive Diagnostics Units

## FEATURES:

- Fully Qualified Bluetooth v2.1 + EDR end product
- CE qualified
- Full modular certification for FCC and IC
- MIC Japan compatibility fully tested with ARIB STD-T66
- TX power:  17 dBm
- RX sensitivity: -94 dBm
- Integrated chip antenna, RF pin or U.FL antenna connector
- Class 1, range up to 650 meters with chip antenna or up to 1km with an external dipole
- Industrial temperature range from -40°C to +85°C
- RoHS Compliant
- USB interface (USB 2.0 compatible)
- UART with bypass mode
- 6 x GPIO
- 1 x 8-bit AIO
- Integrated iWRAP™ Bluetooth stack or HCI firmware

# 1  Ordering Information

| Firmware | U.FL Connector | Internal chip antenna |
|---|---|---|
| iWRAP 5.6 firmware | WT41u-E-AI56 | WT41u-A-AI56 |
| iWRAP 5.5 firmware | WT41u-E-AI55 | WT41u-A-AI55 |
| iWRAP 5.0.2 firmware | WT41u-E-AI5 | WT41u-A-AI5 |
| HCI firmware, BT2.1 + EDR | WT41u-E-HCI21 | WT41u-A-HCI21 |

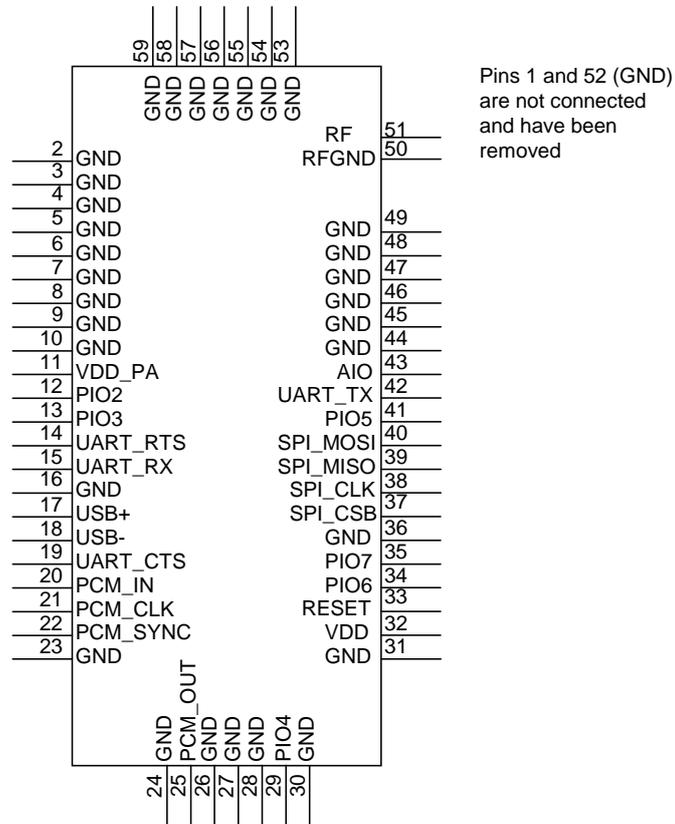**Table 1: Ordering information**

# 2 Pinout and Terminal Description



Pins 1 and 52 (GND) are not connected and have been removed

**Figure 1: WT41u pin out**

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| Pad name | Pad number | Pad type | Description |
|---|---|---|---|
| NC | 1, 52 | Not connected | Pins 1 and 52 are not present on the footprint |
| RESET | 33 | Digital input | Active low reset with weak internal pull-up. Keep low for >5ms to reset module |
| GND | 2-10, 16, 23, 24, 26-28, 30, 31, 36, 44-49, 53-59 | Ground | Ground pads should all be connected to a ground plane with minimum trace length, especially on the antenna end of the module |
| RF | 51 | Not connected | No internal connection |
| RFGND | 50 | Ground | Connect to ground plane |
| VDD_PA | 11 | Supply voltage | Supply voltage for the RF power amplifier and low noise amplifier |
| VDD | 32 | Supply voltage | Supply voltage for the Bluetooth chipset |

**Table 2: Supply and RF Terminal Descriptions**

| PIO signal | Pad number | Description |
|---|---|---|
| PIO[2] | 12 | Bi-directional digital in/out with programmable strength and pull-up/pull-down |
| PIO[3] | 13 | Bi-directional digital in/out with programmable strength and pull-up/pull-down |
| PIO[4] | 29 | Bi-directional digital in/out with programmable strength and pull-up/pull-down |
| PIO[5] | 41 | Bi-directional digital in/out with programmable strength and pull-up/pull-down |
| PIO[6] | 34 | Bi-directional digital in/out with programmable strength and pull-up/pull-down |
| PIO[7] | 35 | Bi-directional digital in/out with programmable strength and pull-up/pull-down |
| AIO[1] | 43 | Bi-directional analog in/out |

**Table 3: GPIO Terminal Descriptions**

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| PCM signal | Pad number | Pad type | Description |
|---|---|---|---|
| PCM_OUT | 25 | Output, weak internal pull-down | Synchronous data output |
| PCM_IN | 20 | Input, weak internal pull-down | Synchronous data input |
| PCM_SYNC | 22 | Bi-directional, weak internal pull-down | Synchronous data sync |
| PCM_CLK | 21 | Bi-directional, weak internal pull-down | Synchronous data clock |

**Table 4: PCM Terminal Descriptions**

| UART signal | Pad number | Pad type | Description |
|---|---|---|---|
| UART_TX | 42 | Output, weak internal pull-up | UART data output, active high |
| UART_RTS# | 14 | Output, weak internal pull-up | UART request to send, active low |
| UART_RX | 15 | Input, weak internal pull-down | UART data input, active high |
| UART_CTS# | 19 | Input, weak internal pull-down | UART clear to send, active low |

**Table 5: UART Terminal Descriptions**

| USB signal | Pad number | Pad type | Description |
|---|---|---|---|
| USB+ | 17 | Bidirectional | USB data line with internal 1.5kohm pull-up |
| USB- | 18 | Bidirectional | USB data line |

**Table 6: USB Terminal Descriptions**

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| SPI signal | Pad number | Pad type | Description |
|---|---|---|---|
| SPI_MOSI | 40 | Input, weak internal pull-down | SPI data input |
| SPI_CS# | 37 | Input, weak internal pull-up | Chip select, active low |
| SPI_CLK | 38 | Input, weak internal pull-down | SPI clock |
| SPI_MISO | 39 | Output, weak internal pull-down | SPI data output |

**Table 7: Terminal Descriptions**

# 3 Electrical Characteristics

## 3.1 Absolute Maximum Ratings

| Specification | Min | Max | Unit |
|---|---|---|---|
| Storage temperature | -40 | 85 | °C |
| VDD_PA, VDD | -0.4 | 3.7 | V |
| Other terminal voltages | VSS-0.4 | VDD+0.4 | V |

**Table 8: Absolute Maximum Ratings**

## 3.2 Recommended Operating Conditions

| Specification | Min | Max | Unit |
|---|---|---|---|
| Operating temperature | -40 | 85 | °C |
| VDD_PA, VDD | 3.0 | 3.6 | V |

**Table 9: Recommended Operating Conditions**

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## 3.3  Input / Output Terminal Characteristics

### 3.3.1  Input/Output Terminal Characteristics (Digital)

| Digital Terminals | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Input Voltage Levels** | | | | | |
| $V_{IL}$ input logic level low | 2.7 V ≤ VDD ≤ 3.0 V | -0.4 | - | 0.8 | V |
| | 1.7 V ≤ VDD ≤ 1.9 V | -0.4 | - | 0.4 | V |
| $V_{IH}$ input logic level high | | 0.7 VDD | - | VDD + 0.4 | V |
| **Output Voltage Levels** | | | | | |
| $V_{OL}$ output logic level low (I$_O$ = 4.0 mA) 2.7V ≤ VDD ≤ 3.0 V | | - | - | 0.2 | V |
| VOL output logic level low (I$_O$ = 4.0 mA) 1.7V ≤ VDD ≤ 1.9 | | - | - | 0.4 | V |
| VOL output logic level high (I$_O$ = 4.0 mA) 2.7V ≤ VDD ≤ 3.0 | | VDD - 0.2 | - | | V |
| VOL output logic level high (I$_O$ = 4.0 mA) 1.7V ≤ VDD ≤ 1.9 | | VDD - 0.4 | - | | V |
| **Input and Tristate Current with** | | | | | |
| Strong pull-up | | -100 | -40 | -10 | µA |
| Strong pull-down | | 10 | 40 | 100 | µA |
| Weak pull-up | | -5.0 | -1.0 | -0.2 | µA |
| Weak pull-down | | 0.2 | 1.0 | 5.0 | µA |
| I/O pad leakage current | | -1 | 0 | 1 | µA |
| $C_I$ input capacitance | | 1.0 | - | 5.0 | pF |

### 3.3.2  Input/Output Terminal Characteristics (USB)

| USB Terminals | Min | Typ | Max | Unit |
|---|---|---|---|---|
| VDD_USB for correct USB operation | 3.1 | | 3.6 | V |
| **Input Threshold** | | | | |
| $V_{IL}$ input logic level log | - | - | 0.3VDD_USB | V |
| $V_{IH}$ input logic level high | 0.7VDD_USB | - | - | V |

## 3.4  PIO Current Sink and Source Capability
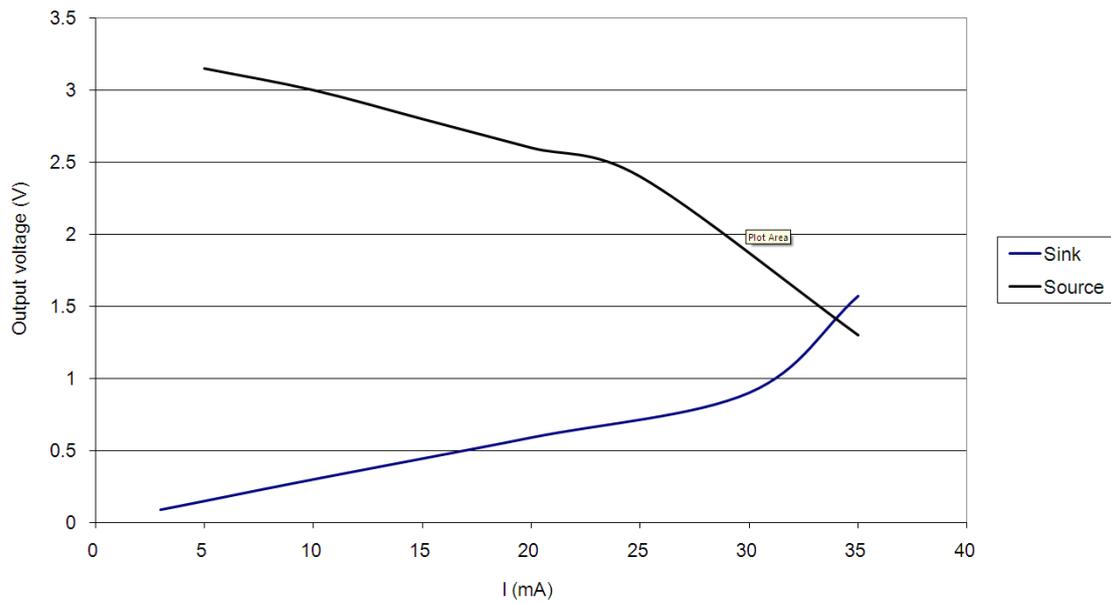


**Figure 2: WT41u PIO Current Drive Capability**

## 3.5  Transmitter Performance For BDR

| RF characteristic | Min | Typ | Max | Bluetooth specification | Unit |
|---|---|---|---|---|---|
| Max transmit power | 16 | 17 | 18 | <20 | dBm |
| Transmit power variation over temperature range | -2 | | 2 | | dB |
| Transmit power variation over supply voltage range | -0.5 | | 0.5 | | dB |
| Transmit power variation over frequency range | -0.5 | | 0.5 | | dB |
| Transmit power control range | -13 | | 17 | | dBm |
| 20dB bandwidth for modulated carrier | | 998 | | <1000 | kHz |
| Avg drift | -11 | | 6 | ±40 | kHz |
| ΔF1avg | | 165 | | 140 to 175 | kHz |

## 3.6 Receiver Performance

Antenna gain not taken into account

| Characteristic, VDD=3.3V, room temperature | Packet type | Typ | Bluetooth specification | Unit |
|---|---|---|---|---|
| Sensitivity for 0.1% BER | DH1 | -94.1 | -70 | dBm |
| | DH5 | -90.5 | | dBm |
| | 2-DH1 | -96.5 | | dBm |
| | 2-DH5 | -94.5 | | dBm |
| | 3-DH1 | -89.5 | | dBm |
| | 3-DH5 | -86 | | dBm |
| Sensitivity variation over temperature range | | +/-2 | | dB |

**Table 10: Receiver sensitivity**

## 3.7 Current Consumption

| Operating mode | Peak | Average | Unit |
|---|---|---|---|
| Stand-by, page mode 0 2000 1 | | 2 | mA |
| TX 3-DH5 | 108 | 85 | mA |
| TX 2-DH5 | 108 | 85 | mA |
| TX DH5 | 184 | 136 | mA |
| RX | 50 | 44 | mA |
| Deep sleep, page mode 0 2000 1 | | 0.36 | mA |
| Inquiry | 113 | 58 | mA |

**Table 11: Current consumption**

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# 4 Physical Dimensions
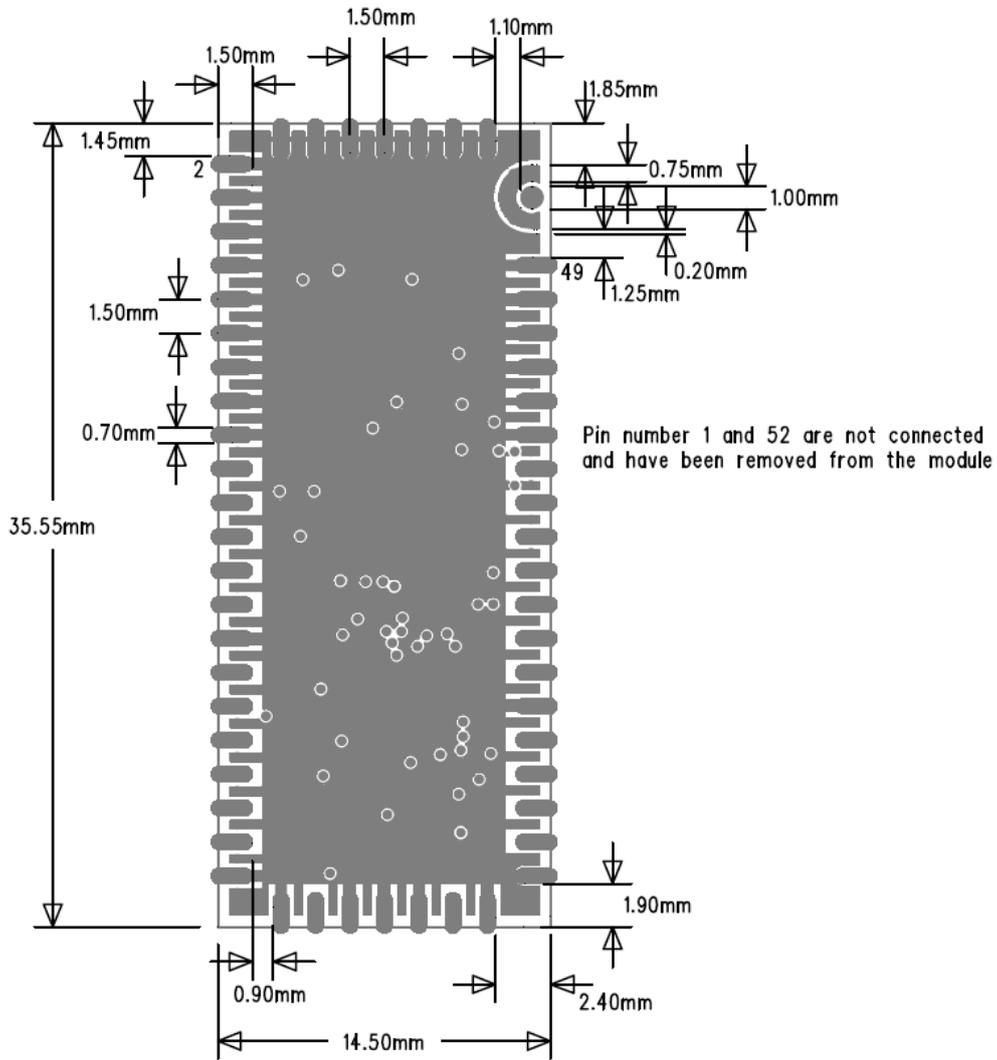


**Figure 3: Physical dimensions (top view)**

Pin number 1 and 52 are not connected and have been removed from the module
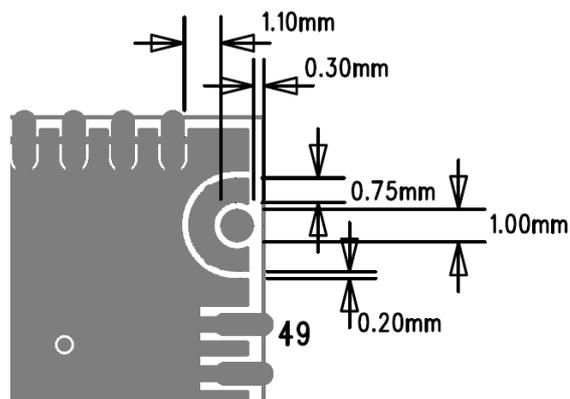


**Figure 4: Dimensions for the RF pin used as antenna connection on WT41u-N (top view)**

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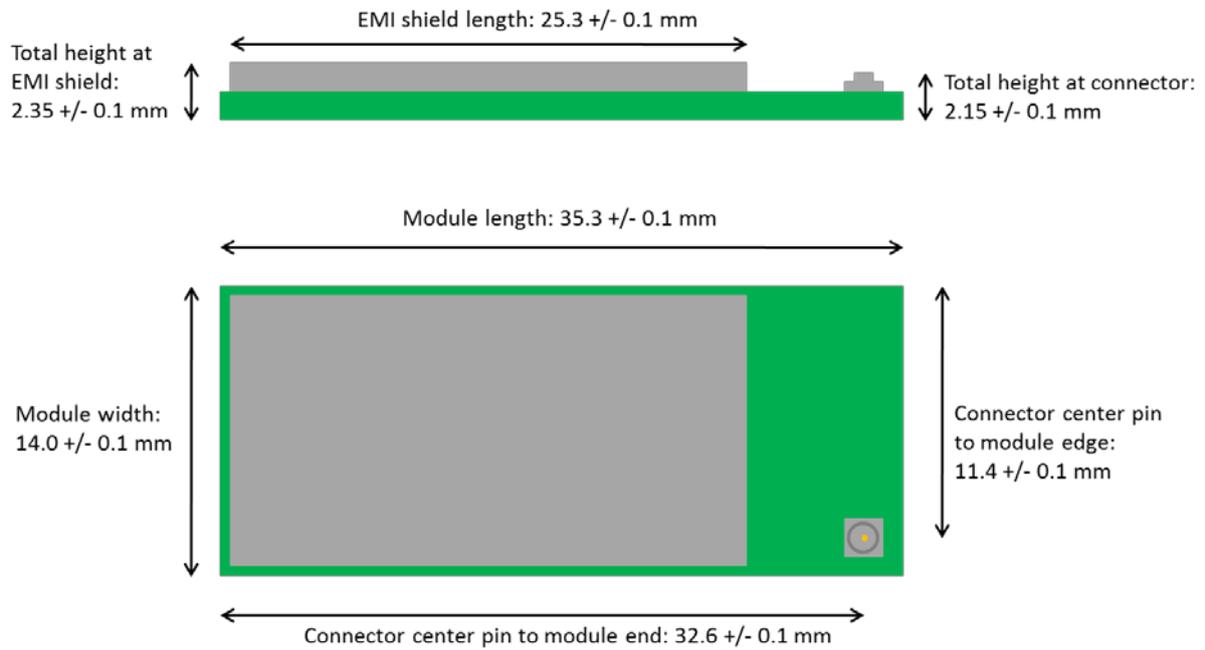
**Figure 5: Dimensions of WT41u-E**
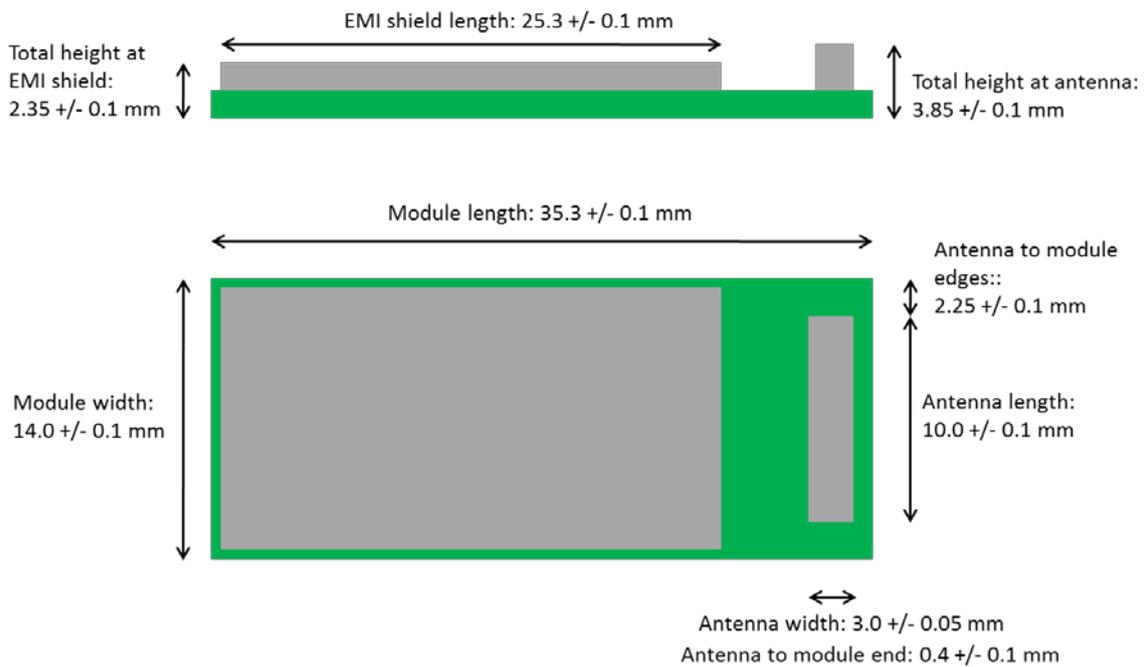


**Figure 6: Dimensions of WT41u-A**

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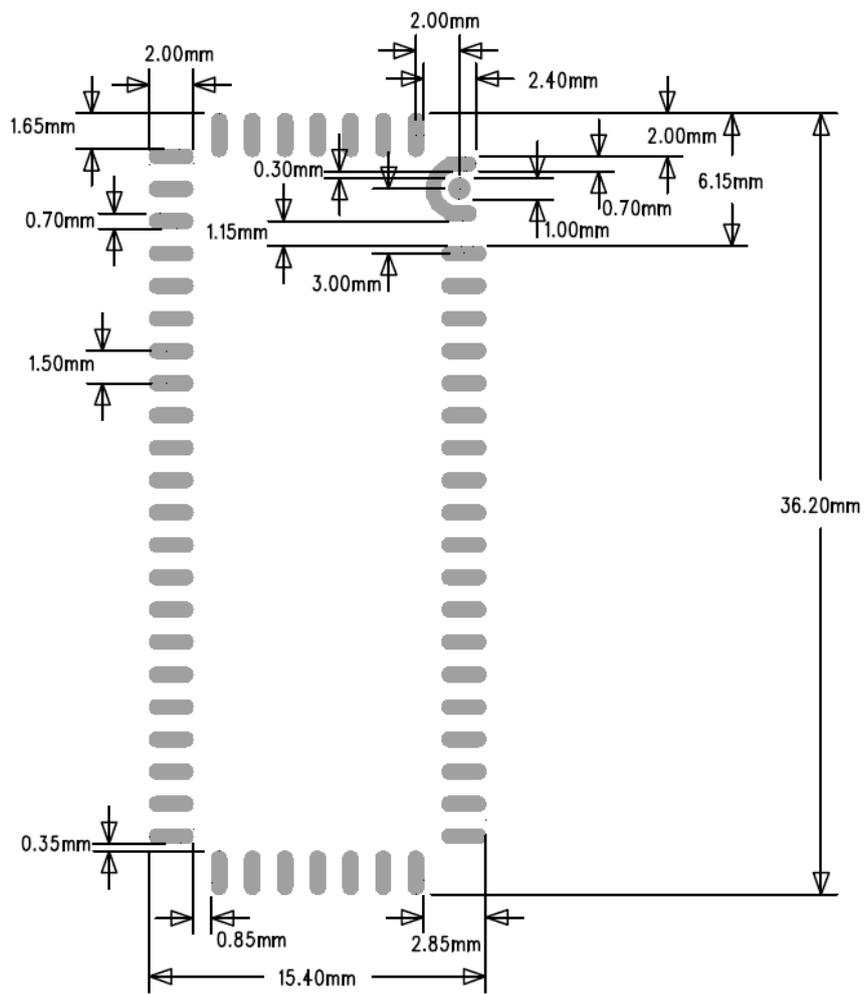
**Figure 7: Recommended land pattern**

# 5 Layout Guidelines

Use good layout practices to avoid excessive noise coupling to supply voltage traces or sensitive analog signal traces, such as analog audio signals. If using overlapping ground planes use stitching vias separated by max 3 mm to avoid emission from the edges of the PCB. Connect all the GND pins directly to a solid GND plane and make sure that there is a low impedance path for the return current following the signal and supply traces all the way from start to the end.

A good practice is to dedicate one of the inner layers to a solid GND plane and one of the inner layers to supply voltage planes and traces and route all the signals on top and bottom layers of the PCB. This arrangement will make sure that any return current follows the forward current as close as possible and any loops are minimized.
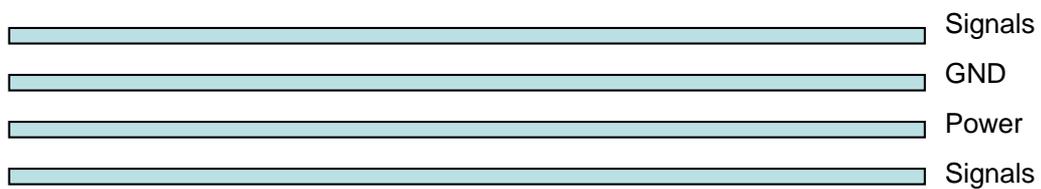


**Figure 8:** Typical 4-layer PCB construction



Overlapping GND layers without GND stitching vias

Overlapping GND layers with GND stitching vias shielding the RF energy

**Figure 9:** Use of stitching vias to avoid emissions from the edges of the PCB

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# 6  UART Interface

This is a standard UART interface for communicating with other serial devices.WT41u UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

Four signals are used to implement the UART function. When WT41u is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD.

UART configuration parameters, such as data rate and packet format, are set using WT41u software.
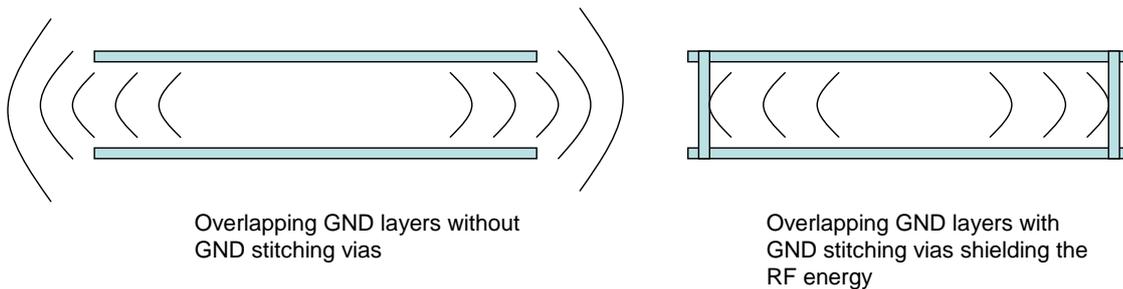

*Note:*

*In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.*


| Parameter | Possible values | |
|---|---|---|
| Data rate | Minimum | 1200bps (2% error) |
| | | 9600bps (1% error) |
| | Maximum | 3Mbps (1% error) |
| Flow control | RTS/CTS or None | |
| Parity | None, Odd or Even | |
| Number of stop bits | 1 or 2 | |
| Bits per channel | 8 | |

**Table 12: Possible UART Settings**


The UART interface is capable of resetting WT41u upon reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 10. If tBRK is longer than the value, defined by PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialise the system to a known state. Also, WT41u can emit a break character that may be used to wake the host.
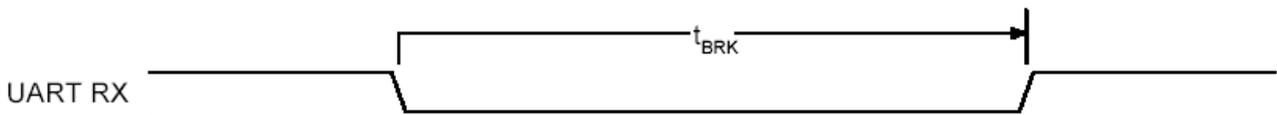


**Figure 10: Break Signal**

Table 17 shows a list of commonly used data rates and their associated values for PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any data rate within the supported range can be set in the PS Key according to the formula in Equation 1.

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$$\text{Data Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

**Equation 1: Data Rate**

| Data rate [bits/s] | Persistent store value (Hex) | Error [bits/s] | Error [%] |
|---|---|---|---|
| 1200 | 0x0005 | 5 | 1.73 |
| 2400 | 0x000A | 10 | 1.73 |
| 4800 | 0x0014 | 20 | 1.73 |
| 9600 | 0x0027 | 39 | -0.82 |
| 19200 | 0x004F | 79 | 0.45 |
| 38400 | 0x009D | 157 | -0.18 |
| 57600 | 0x00EC | 236 | 0.03 |
| 76800 | 0x013B | 315 | 0.14 |
| 115200 | 0x01D8 | 472 | 0.03 |
| 230400 | 0x03B0 | 944 | 0.03 |
| 460800 | 0x075F | 1887 | -0.02 |
| 921600 | 0x0EBF | 3775 | 0 |
| 1382400 | 0x161E | 5662 | -0.01 |
| 1843200 | 0x1D7E | 7550 | 0 |
| 2764800 | 0x2C3D | 11325 | 0 |

**Table 13: Standard Data Rates**

## 6.1 UART Bypass
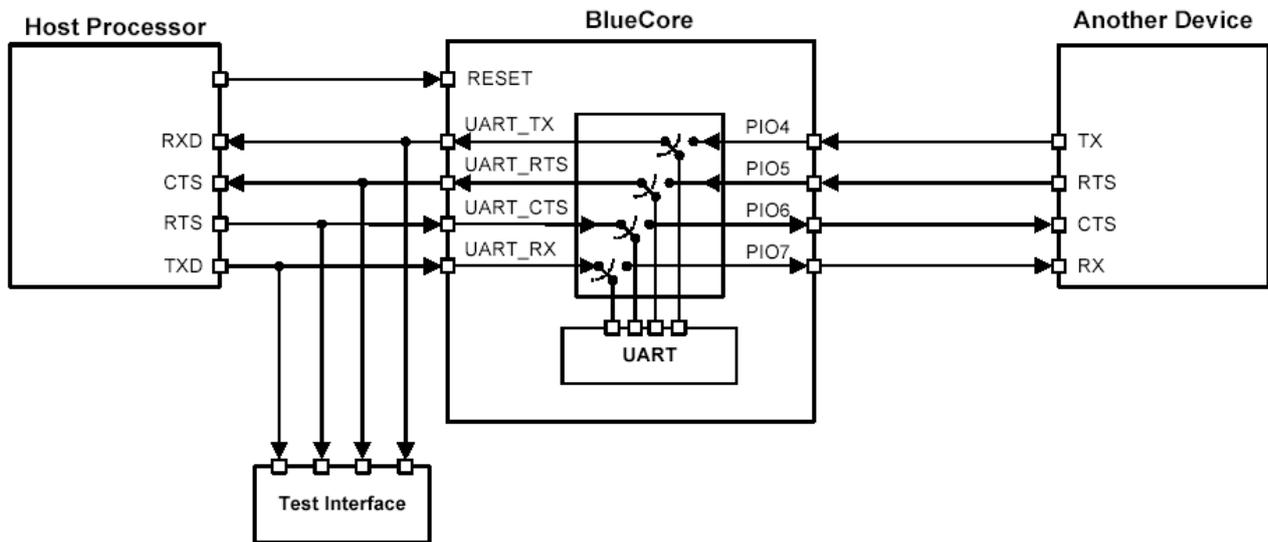


**Figure 11: UART Bypass Architecture**

## 6.2 UART Configuration While Reset is Active

The UART interface for WT41u while the chip is being held in reset is tristate. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tristate when WT41u reset is de-asserted and the firmware begins to run.

## 6.3 UART Bypass Mode

Alternatively, for devices that do not tristate the UART bus, the UART bypass mode on the chipset can be used. The default state of the chipset after reset is de-asserted; this is for the host UART bus to be connected to the chipset UART, thereby allowing communication to the chipset via the UART. All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD.

In order to apply the UART bypass mode, a BCCMD command will be issued to the chipset. Upon this issue, it will switch the bypass to PIO[7:4] as Figure 11 indicates. Once the bypass mode has been invoked, WT41u will enter the Deep Sleep state indefinitely.

In order to re-establish communication with WT41u, the chip must be reset so that the default configuration takes effect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore, it is not possible to have active Bluetooth links while operating the bypass mode.

The current consumption for a device in UART bypass mode is equal to the values quoted for a device in standby mode.

# 7  USB Interface

This is a full speed (12Mbits/s) USB interface for communicating with other compatible digital devices. WT41u acts as a USB peripheral, responding to requests from a master host controller such as a PC.

The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth v2.1 + EDR specification or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

As USB is a master/slave oriented system (in common with other USB peripherals), WT41u only supports USB Slave operation.

## 7.1  USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the the chipset, therefore, have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP/USB_DN and the cable.

## 7.2  USB Pull-Up resistor

WT41u features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when WT41u is ready to enumerate. It signals to the PC that it is a full speed (12Mbits/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ 5% pull-down resistor (in the hub/host) when VDD_PADS = 3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

## 7.3  USB Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD supply terminal must be an absolute minimum of 3.1V. Silicon Labs recommends 3.3V for optimal USB signal quality.

## 7.4  Self-Powered Mode

In self-powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to WT41u via a resistor network ($R_{vb1}$ and $R_{vb2}$), so WT41u can detect when VBUS is powered up. The chipset will not pull USB_DP high when VBUS is off.

Self-powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pullup purposes. A 1.5kΩ 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self-powered mode. The internal pull-up in the chipset is only suitable for bus-powered USB devices, e.g., dongles.
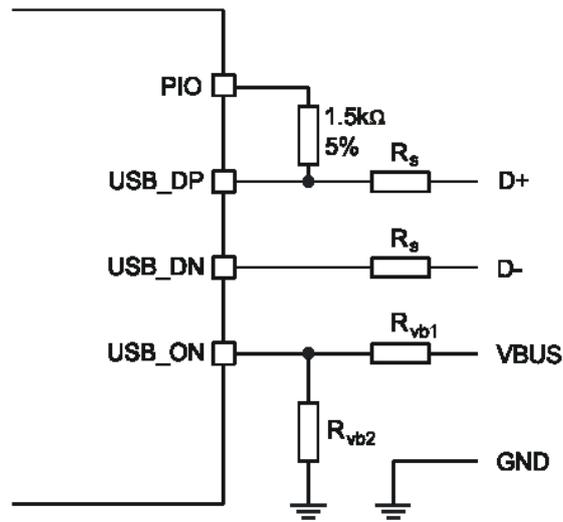
**Figure 12: USB Connections for Self-Powered Mode**

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

| Identifier | Value | Function |
|---|---|---|
| $R_s$ | 27Ω nominal | Impedance matching to USB cable |
| $R_{vb1}$ | 22kΩ 5% | VBUS ON sense divider |
| $R_{vb2}$ | 47kΩ 5% | VBUS ON sense divider |

**Figure 13: USB Interface Component Values**

## 7.5 Bus-Powered Mode

In bus-powered mode, the application circuit draws its current from the 5V VBUS supply on the USB cable. WT41u negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume. On power-up the device must not draw more than 100 mA but after being configured it can draw up to 500 mA.

For WT41u, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA. By default for WT41u the setting is 300 mA.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification. See the USB Specification. Some applications may require soft start circuitry to limit inrush current if more than 10uF is present between VBUS and GND. The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on WT41u supply pins will result in reduced receiver sensitivity and a distorted RF transmit signal.
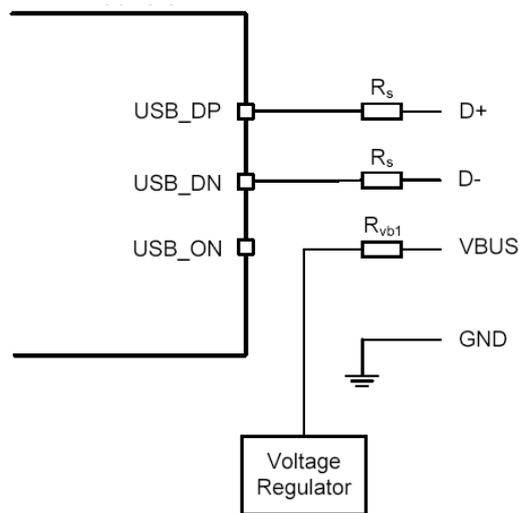
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**Figure 14: USB Connections for Bus-Powered Mode**

## 7.6 USB Suspend Current

All USB devices must permit the USB controller to place them in a USB suspend mode. While in USB Suspend, bus-powered devices must not draw more than 2.5mA from USB VBUS (self-powered devices may draw more than 2.5mA from their own supply). This current draw requirement prevents operation of the radio by bus-powered devices during USB Suspend.

When computing suspend current, the current from VBUS through the bus pull-up and pull-down resistors must be included. The pull-up resistor at the device is 1.5 kΩ. (nominal). The pull-down resistor at the hub is 14.25kΩ. to 24.80kΩ. The pull-up voltage is nominally 3.3V, which means that holding one of the signal lines high takes approximately 200uA, leaving only 2.3mA available from a 2.5mA budget. Ensure that external LEDs and/or amplifiers can be turned off by the chipset. The entire circuit must be able to enter the suspend mode.

## 7.7 USB Detach and Wake-Up Signaling

WT41u can provide out-of-band signaling to a host controller by using the control lines called USB_DETACH and USB_WAKE_UP. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding WT41u into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes WT41u to put USB_DN and USB_DP in high impedance state and turns off the pull-up resistor on DP. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, WT41u will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable) and cannot be sent while the chipset is effectively disconnected from the bus.
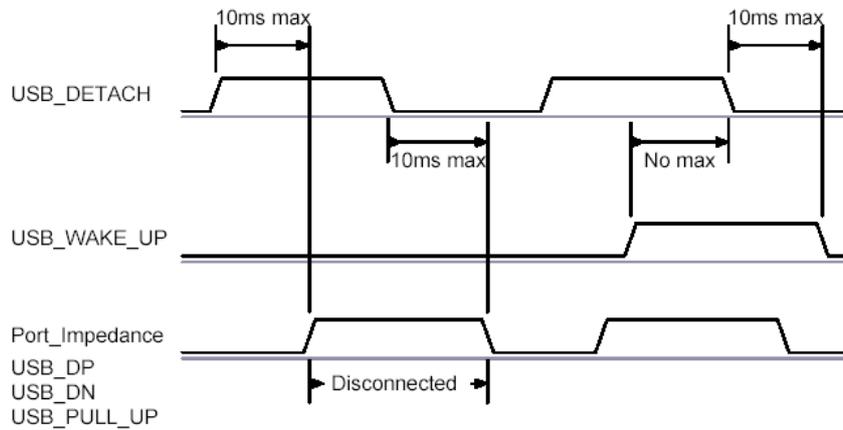
**Figure 15: USB_Detach and USB_Wake_Up Signals**

## 7.8  USB Driver

A USB Bluetooth device driver is required to provide a software interface between the chipset and Bluetooth software running on the host computer. Please, contact Silicon Labs support at http://www.silabs.com for suitable drivers.

## 7.9  USB v2.0 Compliance and Compatibility

Although WT41u meets the USB specification, Silicon Labs cannot guarantee that an application circuit designed around the module is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB Specification v2.0 (Chapter 7) electrical requirements.

The chipset is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

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# 8 Serial Peripheral Interface (SPI)

The SPI port can be used for system debugging. It can also be used for programming the Flash memory and setting the PSKEY configurations. WT41u uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. SPI interface is connected using the MOSI, MISO, CSB and CLK pins.  Please, contact the Silicon Labs support at http://www.silabs.com for detailed information about the instruction cycle.

# 9  PCM Codec Interface

PCM is a standard method used to digitize audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, WT41u has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. WT41u offers a bidirectional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on WT41u allows the data to be sent to and received from a SCO connection. Up to three SCO connections can be supported by the PCM interface at any one time.

WT41u can operate as the PCM interface master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave, it can operate with an input clock up to 2048kHz. WT41u is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit µ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting PSKEY_PCM_CONFIG32.

WT41u interfaces directly to PCM audio devices.

*NOTE: Analog audio lines are very sensitive to RF disturbance. Use good layout practices to ensure noise less audio. Make sure that the return path for the audio signals follows the forward current all the way as close as possible and use fully differential signals when possible. Do not compromise audio routing.*

## 9.1  PCM Interface Master/Slave

When configured as the master of the PCM interface, WT41u generates PCM_CLK and PCM_SYNC.
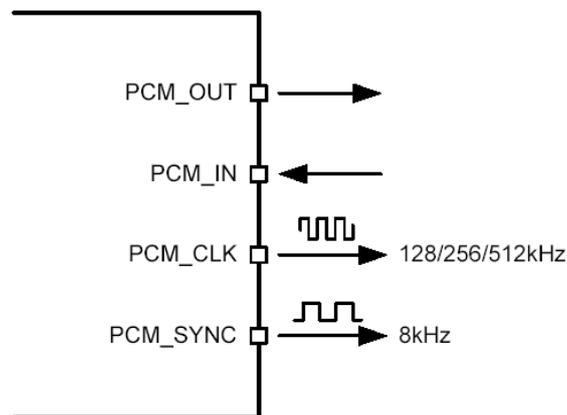


**Figure 16: PCM Interface Master**

When configured as the Slave of the PCM interface, WT41u accepts PCM_CLK rates up to 2048kHz.
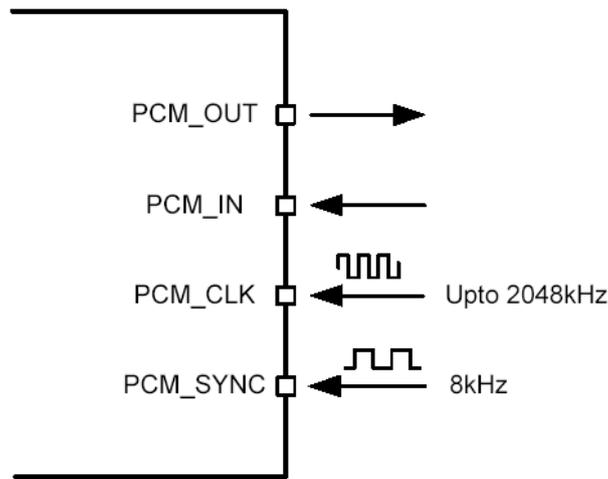
**Figure 17: PCM Interface Slave**

## 9.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When WT41u is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When WT41u is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5s long.
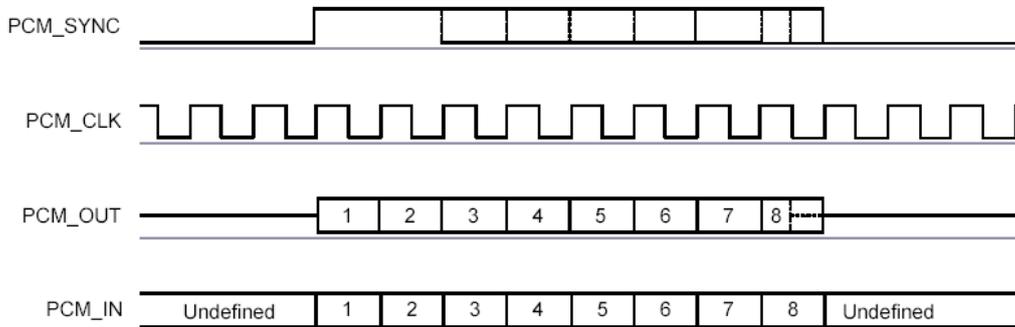


**Figure 18: Long Frame Sync (Shown with 8-bit Companded Sample)**

WT41u samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

## 9.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.
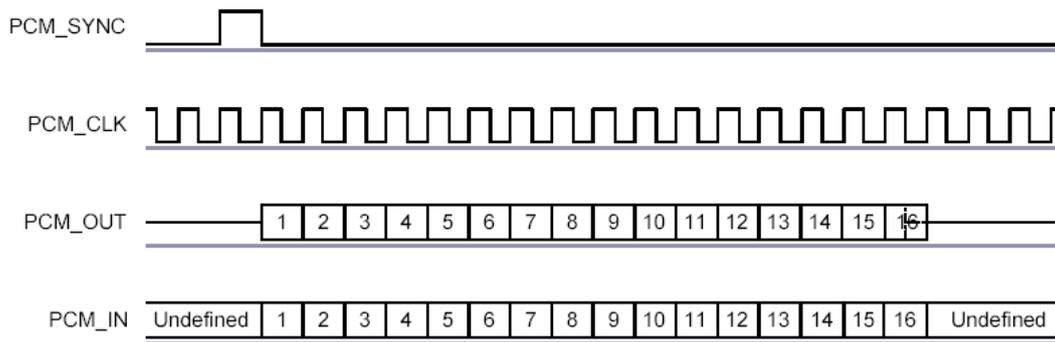
**Figure 19: Short Frame Sync (Shown with 16-bit Sample)**

As with Long Frame Sync, WT41u samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

## 9.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.
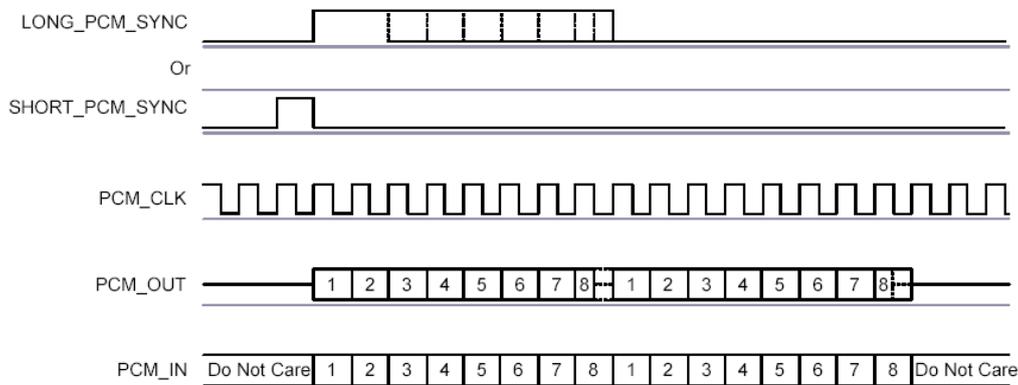


**Figure 20: Multi-slot Operation with Two Slots and 8-bit Companded Samples**

## 9.5 GCI Interface

WT41u is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The two 64kbits/s B channels can be accessed when this mode is configured.
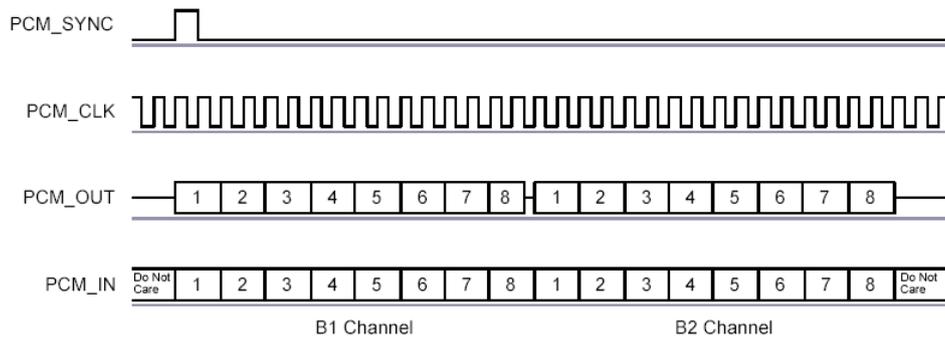
**Figure 21: GCI Interface**

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With WT41u in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

## 9.6  Slots and Sample Formats

WT41u can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

WT41u supports 13-bit linear, 16-bit linear and 8-bit -law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola codecs.

A 16-bit slot with 8-bit companded sample and sign extension selected.

A 16-bit slot with 8-bit companded sample and zeros padding selected.

A 16-bit slot with 13-bit linear sample and sign extension selected.

A 16-bit slot with 13-bit linear sample and audio gain selected.
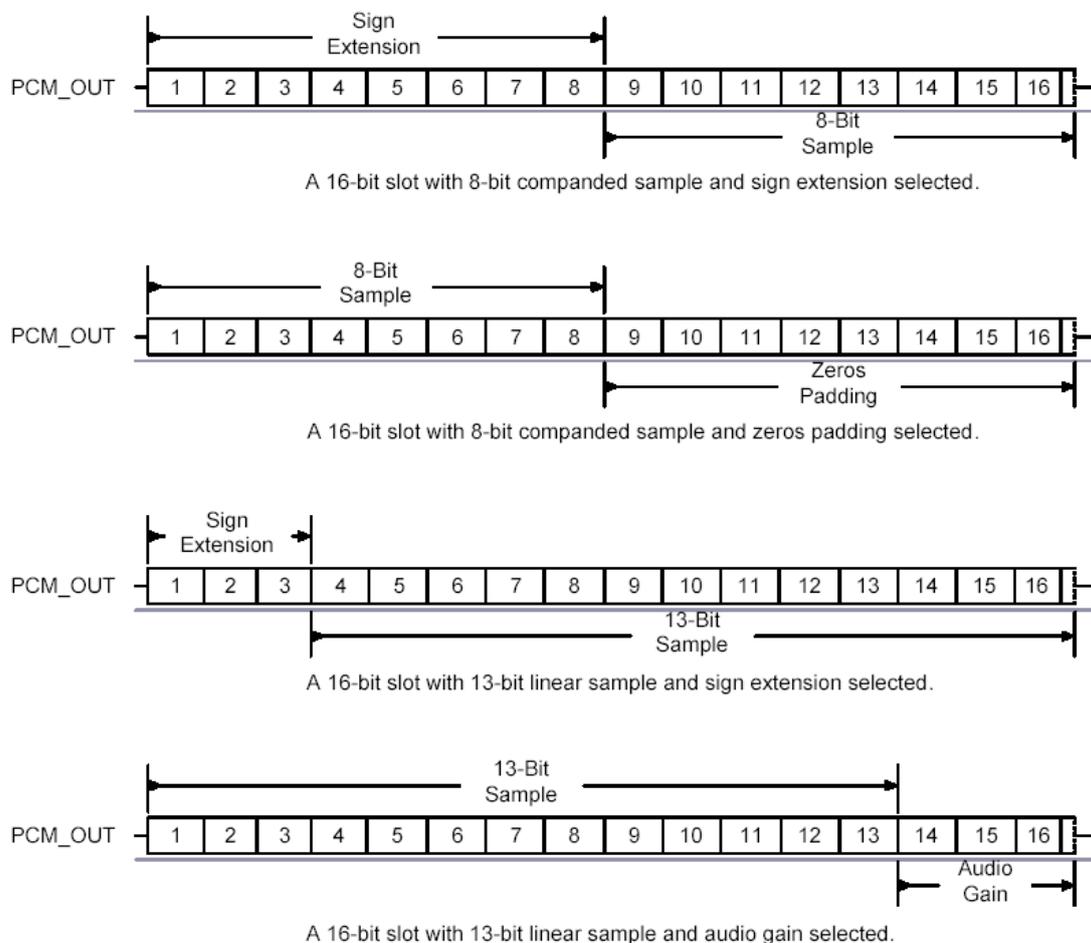
**Figure 22: 16-bit Slot Length and Sample Formats**

## 9.7  Additional Features

WT41u has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some codecs use to control power down.

## 9.8  PCM_CLK and PCM_SYNC Generation

WT41u has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by DDS from the chipset internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). This second method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

The Equation 2 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

**Equation 2: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock**

The frequency of PCM_SYNC relative to PCM_CLK can be set using Equation 3:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

**Equation 3: PCM_SYNC Frequency Relative to PCM_CLK**

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

## 9.9  PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 detailed in Table 18 and PSKEY_PCM_LOW_JITTER_CONFIG in Table 19. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT.

| Name | Bit position | Description |
|---|---|---|
| - | 0 | Set to 0 |
| SLAVE MODE EN | 1 | 0 selects Master mode with internal generation of PCM_CLK and PCM_SYNC. 1 selects Slave mode requiring externally generated PCM_CLK and PCM_SYNC. This should be set to 1 if 48M_PCM_CLK_GEN_EN (bit 11) is set. |
| SHORT SYNC EN | 2 | 0 selects long frame sync (rising edge indicates start of frame), |
| - | 3 | Set to 0 |
| SIGN EXTENDED EN | 4 | 0 selects long frame sync (rising edge indicates start of frame), 1 selects short frame sync (falling edge indicates start of frame). |
| LSB FIRST EN | 5 | 0 transmits and receives voice samples MSB first, 1 uses LSB |
| TX TRISTATE EN | 6 | 0 transmits and receives voice samples MSB first, 1 uses LSB |
| TX TRISTATE RISING EDGE EN | 7 | 0 tristates PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is also not active. 1 tristates PCM_OUT after the rising edge of PCM_CLK. |
| SYNC SUPPRESS EN | 8 | 0 enables PCM_SYNC output when master, 1 suppresses PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilize this to enter a low power state |
| GCI MODE EN | 9 | 1 enables GCI mode. |
| MUTE EN | 10 | 1 forces PCM_OUT to 0. |
| 48M PCM CLK GEN EN | 11 | 0 sets PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock. 1 sets PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock. |
| LONG LENGTH SYNC EN | 12 | 0 sets PCM_SYNC length to 8 PCM_CLK cycles and 1 sets length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1. |
| - | [20:16] | Set to 0b00000. |
| MASTER CLK RATE | [22:21] | Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low. |
| ACTIVE SLOT | [26:23] | Default is 0001. Ignored by firmaware |
| SAMPLE FORMAT | [28:27] | Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration 8 (0b11) bit sample 8 cycle slot duration. |

**Table 14: PSKEY_PCM_CONFIG32 description**

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| Name | Bit position | Description |
| --- | --- | --- |
| CNT LIMIT | [12:0] | Sets PCM_CLK counter limit |
| CNT RATE | [23:16] | Sets PCM_CLK count rate |
| SYNC LIMIT | [31:24] | Sets PCM_SYNC division relative to PCM_CLK |

**Table 15: PSKEY_PCM_LOW_JITTER_CONFIG Description**

# 10 I/O Parallel Ports

Six lines of programmable bidirectional input/outputs (I/O) are provided. All the PIO lines are power from VDD.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset. Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes.

WT41u has a general purpose analogue interface pin AIO[1]. This is used to access internal circuitry and control signals. It may be configured to provide additional functionality.

Auxiliary functions available via AIO[1] include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at this pin include the band gap reference voltage and a variety of clock signals: 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analogue signals, the voltage range is constrained by the analogue supply voltage internally to the module (1.8V). When configured to drive out digital level signals (e.g., clocks), the output voltage level is determined by VDD.

## 10.1 PIO Defaults

Silicon Labs cannot guarantee that these terminal functions remain the same. Refer to the software release note for the implementation of these PIO lines, as they are firmware build-specific.

# 11 Reset

WT41u may be reset from several sources: RESET pin, power on reset, a UART break character or via software configured watchdog timer. The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESET be applied for a period greater than 5ms.

The power on reset occurs when the VDD_CORE supply internally to the module falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V. At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are tri-state.

The reset should be held active at power up until all the supply voltages have stabilized to ensure correct operation of the internal flash memory. Following figure shows an example of a simple power up reset circuit. Time constant of the RC circuitry is set so that the supply voltage is safely stabilized before the reset deactivates.
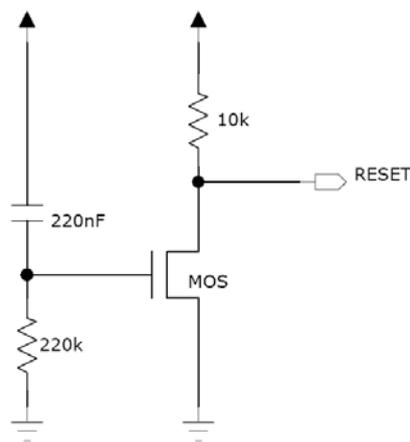
**Figure 23: Example of a simple power on reset circuit.**

## 11.1 Pin States on Reset

| Pad name | State |
|---|---|
| PIO[7:2] | Input, weak pull-down |
| PCM_OUT | 3-state, weak pull-down |
| PCM_IN | Input, weak pull-down |
| PCM_SYNC | Input, weak pull-down |
| PCM_CLK | Input, weak pull-down |
| UART_TX | 3-state, weak pull-up |
| UART_RX | Input, weak pull-down |
| UART_RTS | 3-state, weak pull-up |
| UART_CTS | Input, weak pull-down |
| USB+ | Input, weak pull-down |
| USB- | Input, weak pull-down |
| SPI_CSB | Input, weak pull-down |
| SPI_CLK | Input, weak pull-down |
| SPI_MOSI | Input, weak pull-down |
| SPI_MISO | 3-state, weak pull-down |
| AIO[1] | Output, driving low |

**Table 16: Pin States on Reset**

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# 12 Certifications

## 12.1 Bluetooth

The WT41u is Bluetooth qualified and the declaration ID is D032265 (QDID 88818)

## 12.2 FCC

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and

2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user's authority to operate the equipment.

**FCC RF Radiation Exposure Statement:**

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter meets both portable and mobile limits as demonstrated in the RF Exposure Analysis. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures. As long as the condition above is met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

**OEM Responsibilities to comply with FCC Regulations**

The WT41u Module has been certified for integration into products only by OEM integrators under the following condition:

- The antenna(s) must be installed such that a minimum separation distance of 42 mm is maintained between the radiator (antenna) and all persons at all times.

- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

As long as the conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

**Note:** In the event that this condition cannot be met (for certain configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

**End Product Labeling**

The WT41u Module is labeled with its own FCC ID. If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

**"Contains Transmitter Module FCC ID: QOQWT41u"**

or

**"Contains FCC ID: QOQWT41u"**

The OEM integrator must not provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

## 12.3 ISEDC

This radio transmitter (IC: 5123A-WT41U) has been approved by Industry Canada to operate with the embedded chip antenna. Other antenna types are strictly prohibited for use with this device.

This device complies with Industry Canada's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference; and

2. This device must accept any interference, including interference that may cause undesired operation of the device.

**RF Exposure Statement**

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5. WT41u meets the given requirements when the minimum separation distance to human body 40 mm. RF exposure or SAR evaluation is not required when the separation distance is 40 mm or more. If the separation distance is less than 40 mm the OEM integrator is responsible for evaluating the SAR.

OEM Responsibilities to comply with IC Regulations The WT41u Module has been certified for integration into products only by OEM integrators under the following conditions:

• The antenna(s) must be installed such that a minimum separation distance of 40 mm is maintained between the radiator (antenna) and all persons at all times.

• The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

**Note**: In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the IC authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate IC authorization.

**End Product Labeling**

The WT41u module is labeled with its own IC ID. If the IC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

**"Contains Transmitter Module IC: 5123A-WT41u"**

or

**"Contains IC: 5123A-WT41u"**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

## 12.3.1    ISEDC (Français)

Cet émetteur radio (IC : 5123A-WT41u) a reçu l'approbation d'Industrie Canada pour une exploitation avec l'antenne puce incorporée. Il est strictement interdit d'utiliser d'autres types d'antenne avec cet appareil.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage; et

2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible de provoquer un fonctionnement non désiré de l'appareil.

**Déclaration relative à l'exposition aux radiofréquences (RF)**

Les limites applicables à l'exemption de l'évaluation courante du DAS sont énoncées dans le CNR 102, 5e édition. Le module Bluetooth WT41u répond aux exigences données quand la distance de séparation minimum par rapport au corps humain est de 40 mm. L'évaluation de l'exposition aux RF ou du DAS n'est pas requise quand la distance de séparation est de 40 mm ou plus. Si la distance de séparation est inférieure à 40 mm, il incombe à l'intégrateur FEO d'évaluer le DAS.

**Responsabilités du FEO ayant trait à la conformité avec les règlements IC**

Le Module Bluetooth WT41u a été certifié pour une intégration dans des produits uniquement par les intégrateurs FEO dans les conditions suivantes:

• La ou les antennes doivent être installées de telle façon qu'une distance de séparation minimum de 40 mm soit maintenue entre le radiateur (antenne) et toute personne à tout moment.

• Le module émetteur ne doit pas être installé au même endroit ou fonctionner conjointement avec toute autre antenne ou émetteur.

Dès lors que les deux conditions ci-dessus sont respectées, aucun test supplémentaire de l'émetteur n'est obligatoire. Cependant, il incombe toujours à l'intégrateur FEO de tester la conformité de son produit final vis-à-vis de toute exigence supplémentaire requise avec ce module installé (par exemple, émissions de dispositifs numériques, exigences relatives aux matériels périphériques PC, etc).

**Note:** S'il s'avère que ces conditions ne peuvent être respectées (pour certaines configurations ou la colocation avec un autre émetteur), alors l'autorisation IC n'est plus considérée comme valide et l'identifiant IC ne peut plus être employé sur le produit final. Dans ces circonstances, l'intégrateur FEO aura la responsabilité de réévaluer le produit final (y compris l'émetteur) et d'obtenir une autorisation IC distincte.

**Étiquetage du produit final**

L'étiquette du Module WT41u porte son propre identifiant IC. Si l'identifiant IC n'est pas visible quand le module est installé à l'intérieur d'un autre appareil, alors l'extérieur de l'appareil dans lequel le module est installé doit aussi porter une étiquette faisant référence au module qu'il contient. Dans ce cas, une étiquette comportant les informations suivantes doit être apposée sur une partie visible du produit final.

**"Contient le module émetteur IC: 5123A-WT41U"**

ou

**"Contient IC : 5123A-WT41U"**

L'intégrateur FEO doit être conscient de ne pas fournir d'informations à l'utilisateur final permettant d'installer ou de retirer ce module RF ou de changer les paramètres liés aux RF dans le mode d'emploi du produit final.

## 12.4 CE

The Declaration of Compliance and the test documentation can be consulted in www.silabs.com.

Please note that every application using the WT41-A or WT41-N will need to perform the radio EMC tests on the end product according to EN 301 489-17.

RF exposure requirements must be verified in an end product assembly.

Test documentation and software for the EN 300 328 radiated spurious emissions testing can be requested from the Silicon Labs support.

## 12.5 MIC Japan

The WT41u module in certified for Japan. Certification number: 209-J00231 Since September 1, 2014 it is allowed (and highly recommended) that a manufacturer who integrates a radio module in their host equipment can place the certification mark and certification number (the same marking/number as depicted on the label of the radio module) on the outside of the host equipment. The certification mark and certification number must be placed close to the text in the Japanese language which is provided below. This change in the Radio Law has been made in order to enable users of the combination of host and radio module to verify if they are actually using a radio device which is approved for use in Japan.

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation: "This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law."

## 12.6 Qualified Antenna Types for WT41u-E and WT41u-N

This device has been designed to operate with a standard 2.14 dBi dipole antenna. Any antenna of a different type or with a gain higher than 2.14 dBi is strictly prohibited for use with this device. Using an antenna of a different type or gain more than 2.14 dBi will require additional testing for FCC, CE and IC. The required antenna impedance is 50 Ω.

| Antenna type | Maximum gain |
|---|---|
| Dipole | 2.14 dBi |

**Table 17:** Qualified Antenna Types for WT41u-E/N

To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (EIRP) is not more than that permitted for successful communication.

Any standard 2.14 dBi dipole antenna can be used without an additional application to FCC.
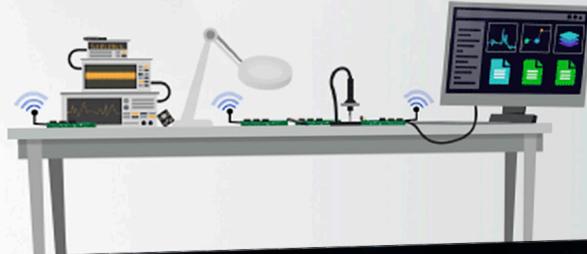
## 12.7 Moisture Sensitivity Level (MSL)

Moisture sensitivity level (MSL) of this product is 3. For the handling instructions please refer to JEDEC J-STD-020 and JEDEC J-STD-033.

If baking is required, devices may be baked for 12 hours at 125°C +/-5°C for high temperature device containers.

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